

G41T-M2


Ver. 1.0

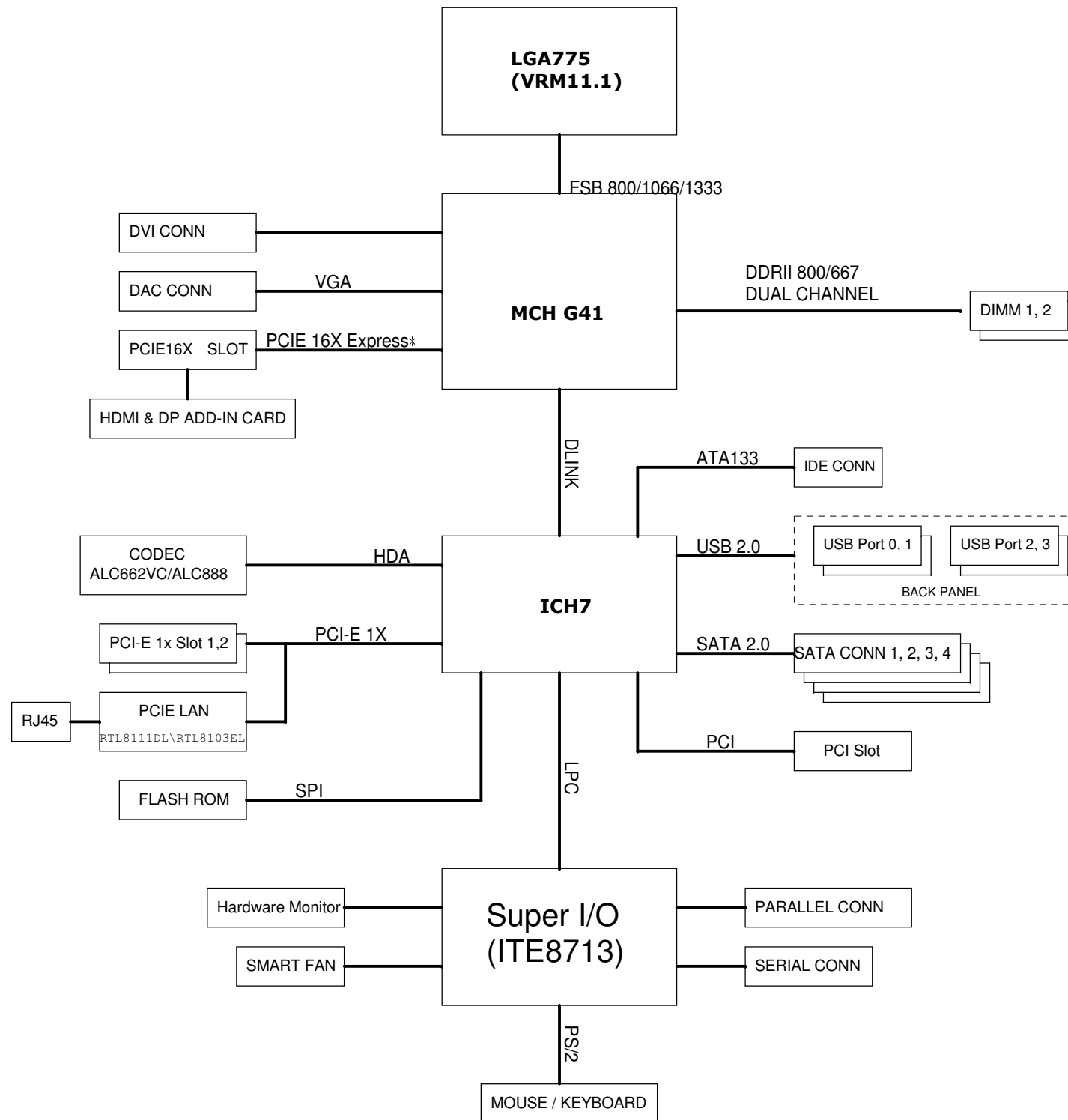
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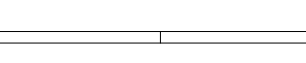
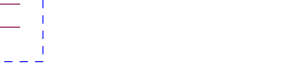
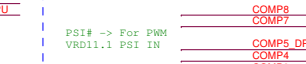
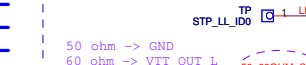
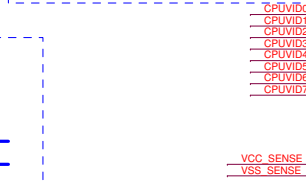
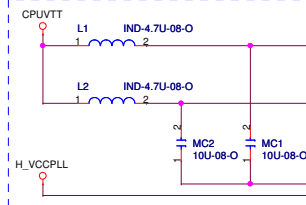
History :

Ver A :	2009/03/24	Add DVI Function. p.22
	2009/03/31	Add Support Codec HDMI Sound Output. p6 & p.11
	2009/04/20	Change CLK Gen to ICS9LPRS525. p.12
	2009/04/30	Jeff TU Modify R302 => 15k ,R286 =>30k ,R292 =>1.5k for uP6206 . p.17
	2009/05/04	Ken Modify R511 => 16k OCP for RT9214 . p.27
	2009/05/06	Modify R58 , R59=> 100 ohm to fixed V/Hsync overshoot . p.17
		Modify BC82~BC => 6.8p to fixed R.G.B Rise time . p.17
		Modify FB13~FB15 => 60ohm to fixed R.G.B noise . p.17
		Modify FB5 to 2.2ohm , add MC88 10u for DAC voltage. p.17
	2009/05/07	Add BC119 ,BC96 ,BC94 0.1u, RN63.64 commond choke 90ohm for EMI. p22

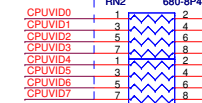
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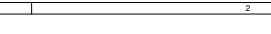
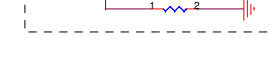
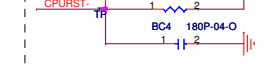
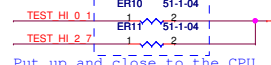
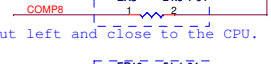
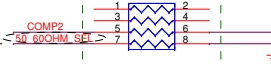
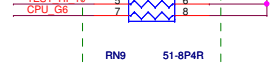
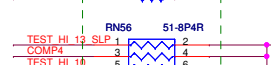
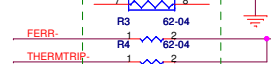
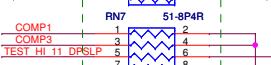
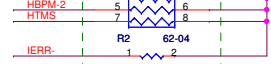
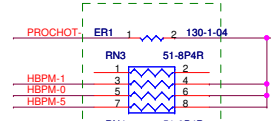
Close to CPU 12-mil width minimum



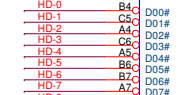
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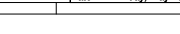
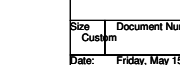
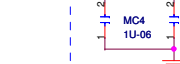
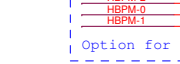
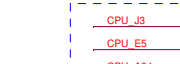
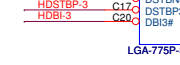
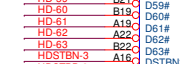
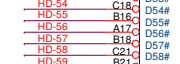
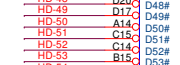
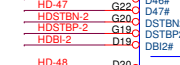
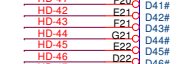
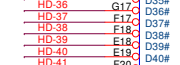
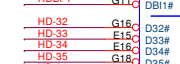
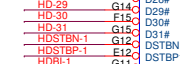
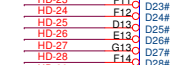
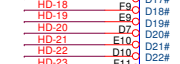
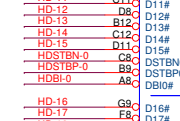
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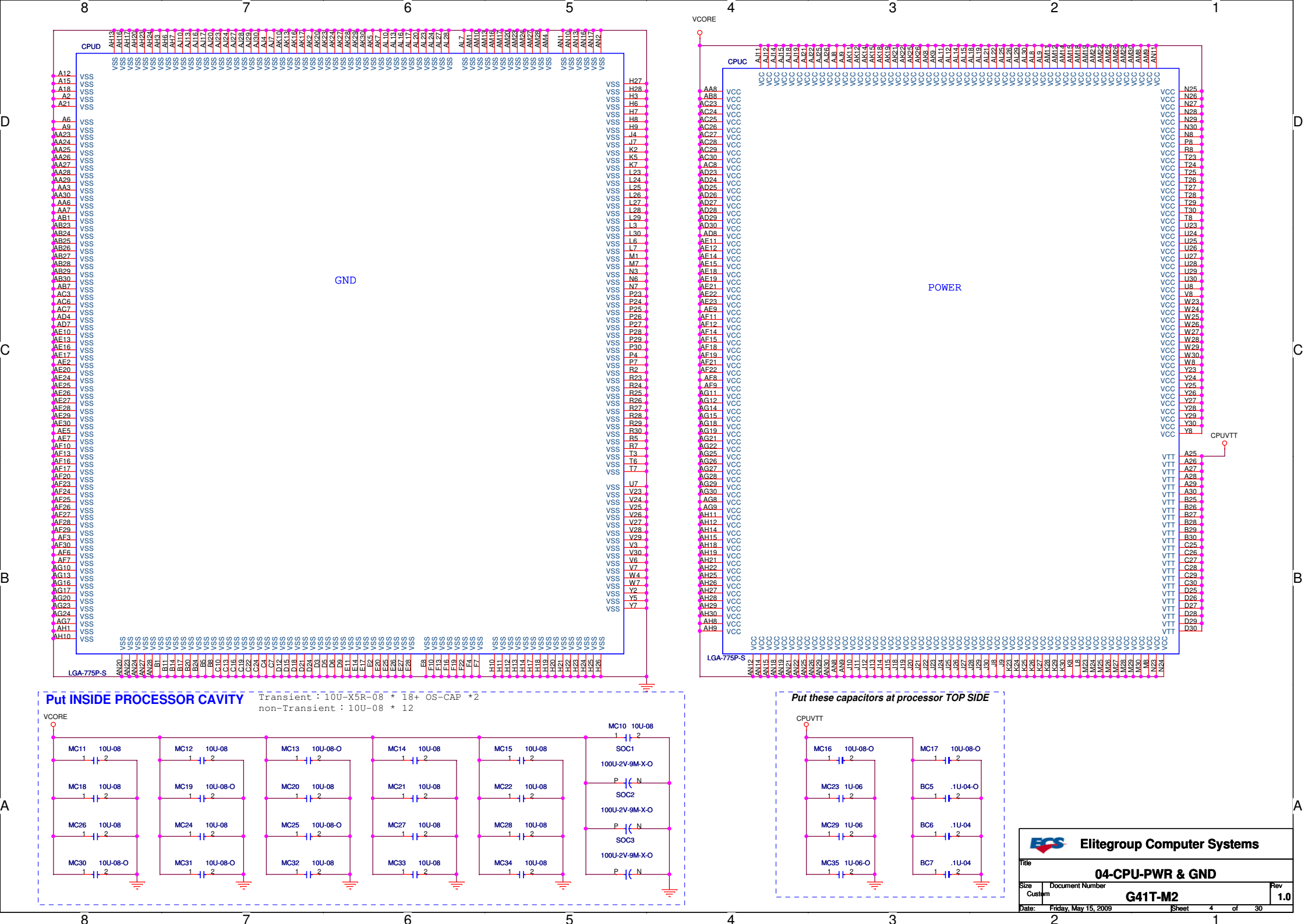


Close to CPU.

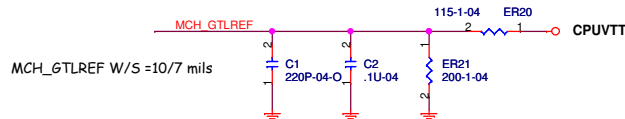
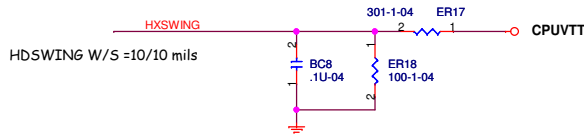
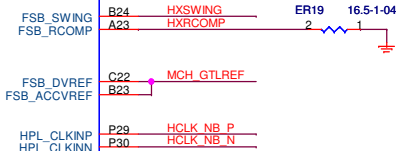
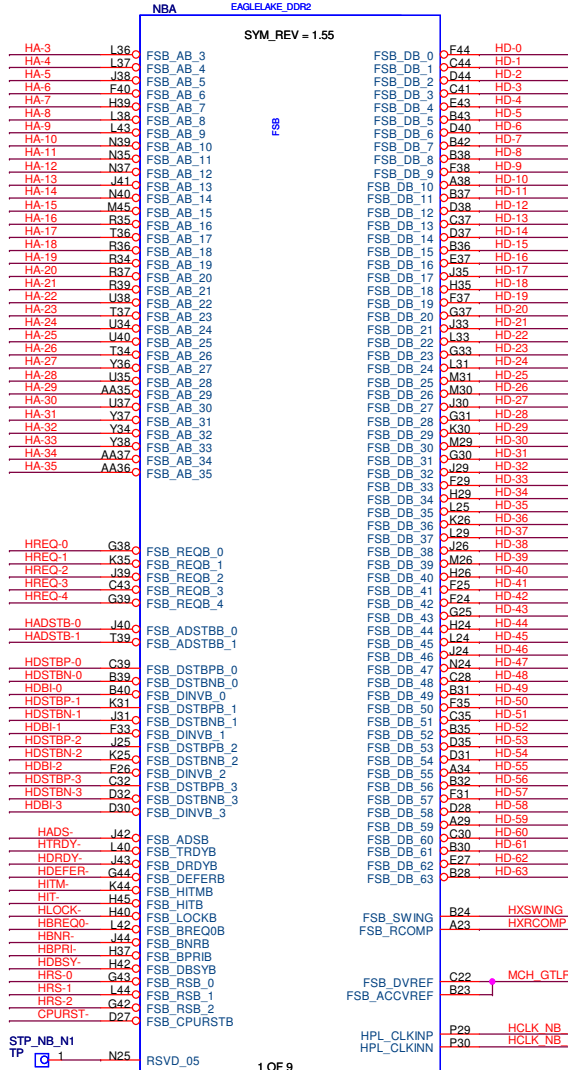
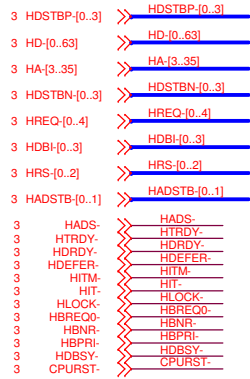


Put left and close to the CPU.





HOST

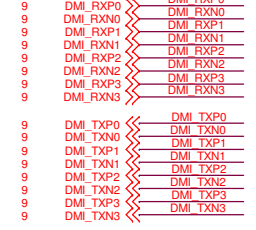




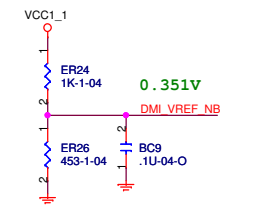
Sequence



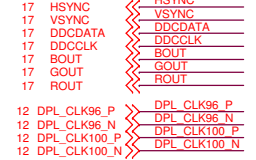
DMI Link



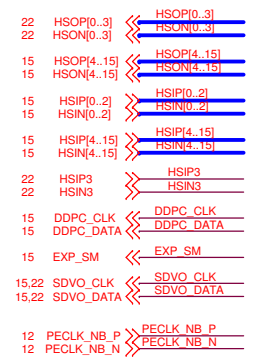
Control Link



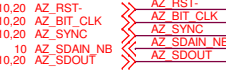
VGA DAC



PCIEx16



HDA



For G41 Only :

CL_CLK and CL_DATA No Connect

CL_RST# Connect to PLTRST#

CL_VREF achieve 0.352 reference voltage

CL_PWROK Connect to PWOK

VCC_CL Connect to 1.1V GMCH core voltage

TPM1.2 STRAPS TABLE

	ENABLE	DISABLE	DESCRIPTION
ETPM	L	Floating	TPM1.2 on MCH In MCH Pin.L17
SPIDO	H	Floating	TPM1.2 on ICH10 In ICH10 Pin.C26
TPM_PP	H	L	TPM Physical Presence In ICH Pin.C12

GMCH STRAPS TABLE

	H	L	DESCRIPTION
EXP_SLR	NORMAL/ ATX	REVERSE/ BTX	PCI EXPRESS STATIC LANE REVERSAL
EXP_SM	CONCURRENT	NON-CONCURRENT	PCI EXPRESS / SDVO COEXISTENCE
TCEN	ENABLE	DISABLE	TLS CONFIDENTIALITY



Elitegroup Computer Systems

Title: 06-G43/G41_DMI/PCIE/DAC/HDMI

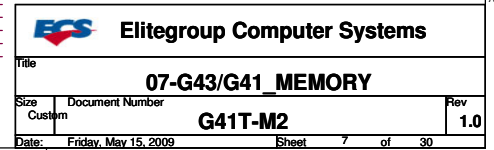
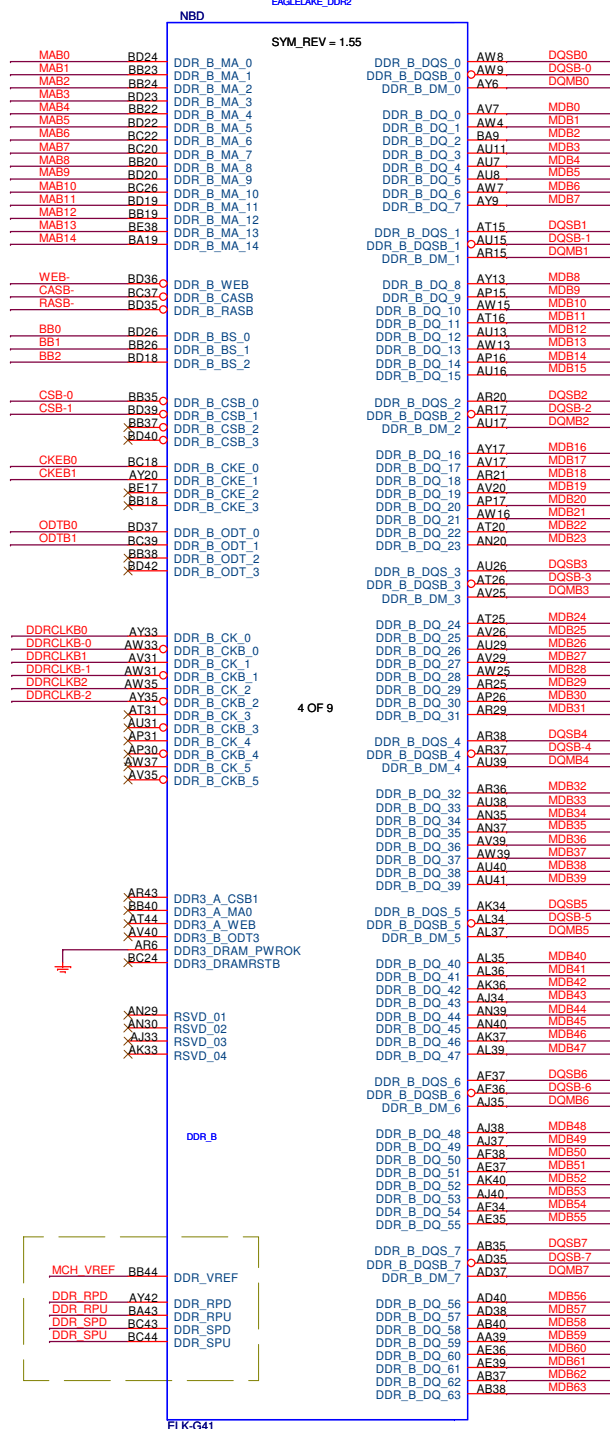
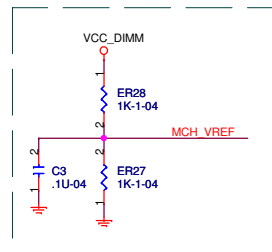
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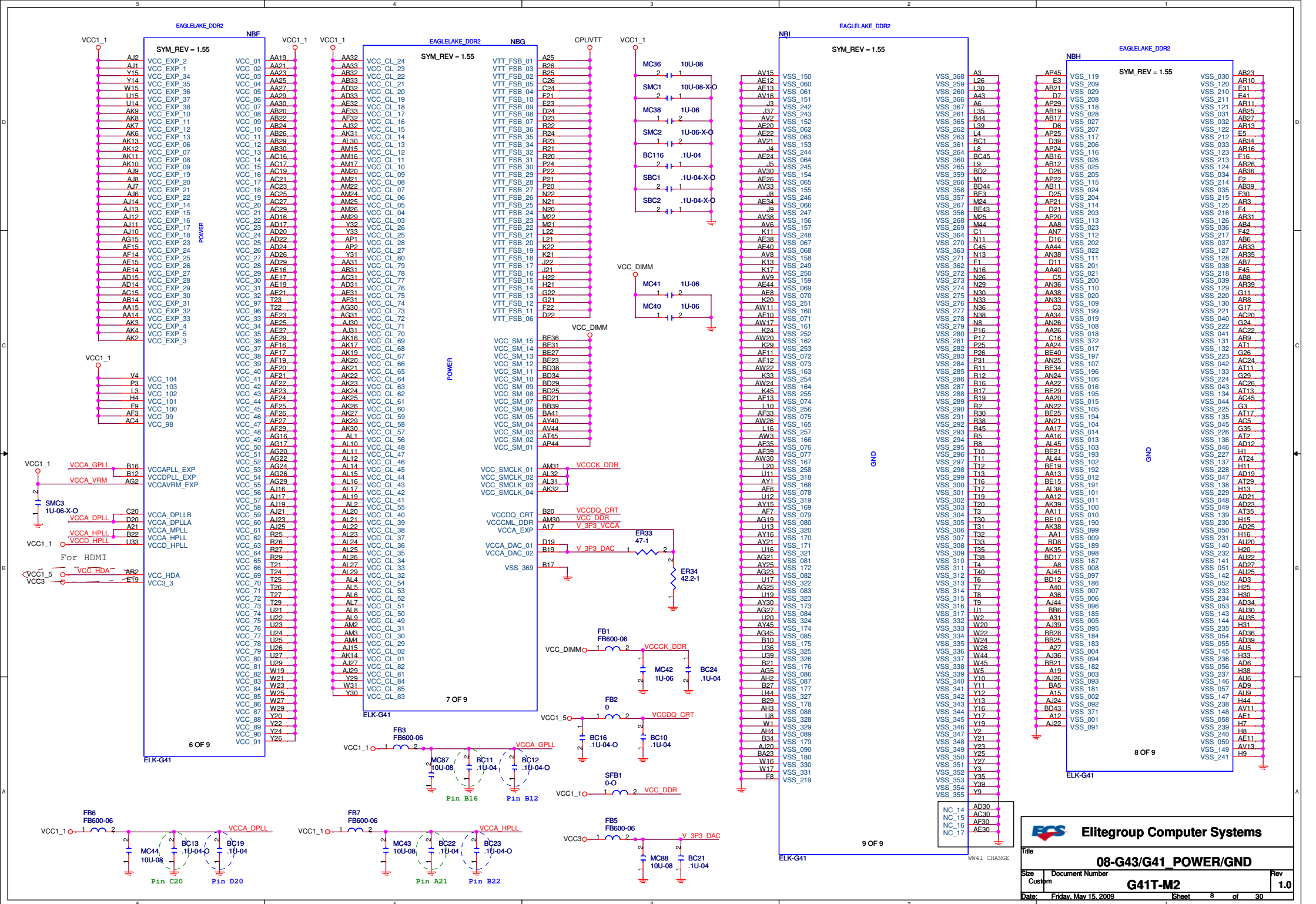
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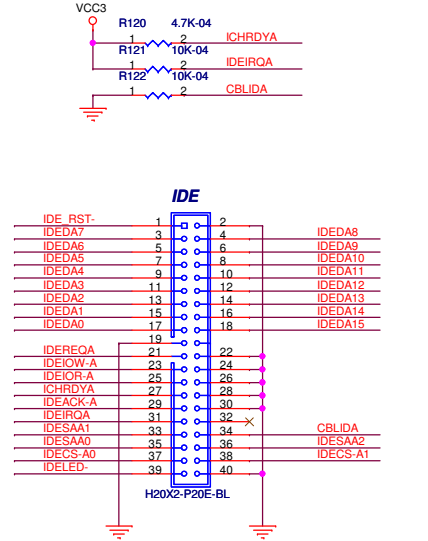
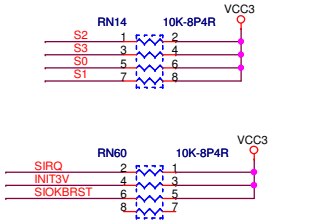
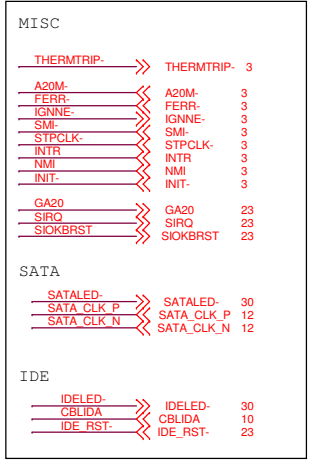
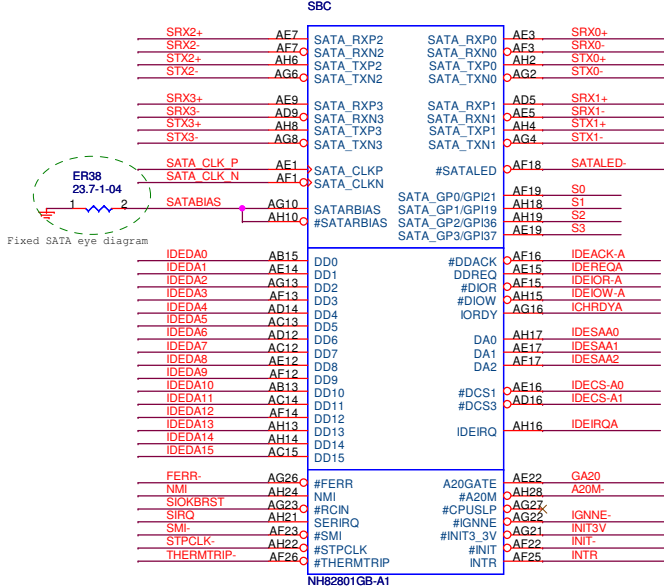
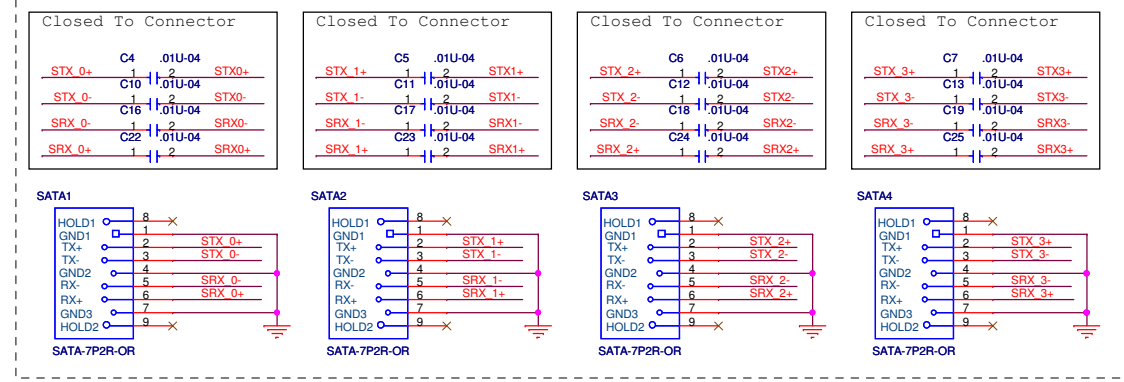
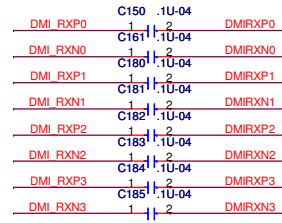
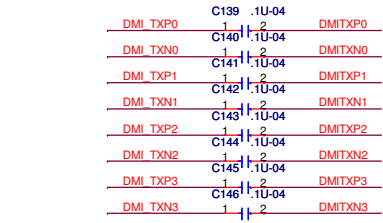
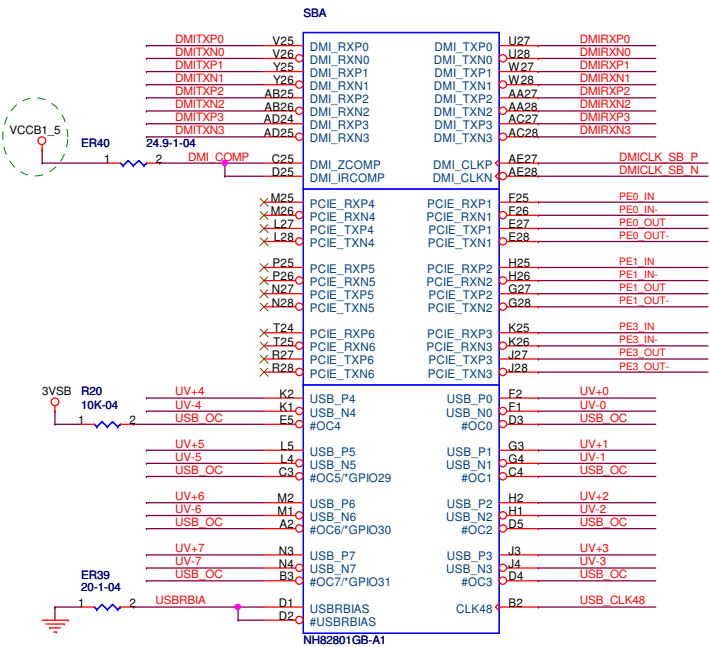
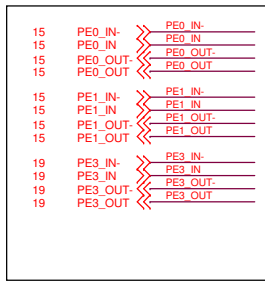
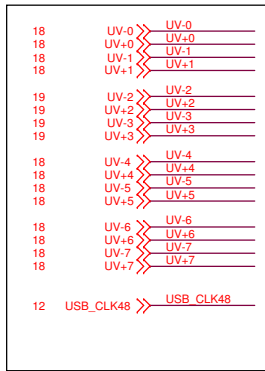
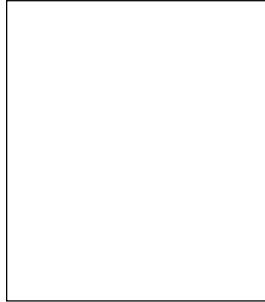
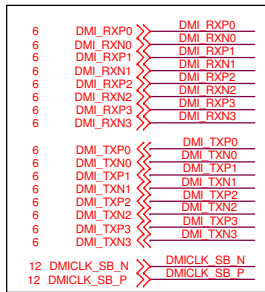
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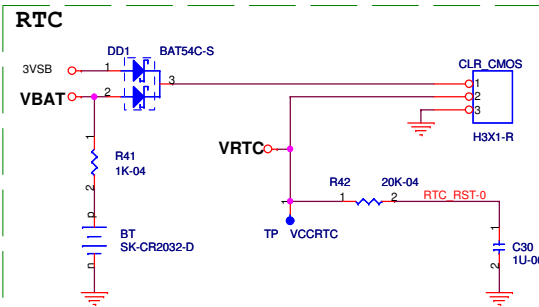
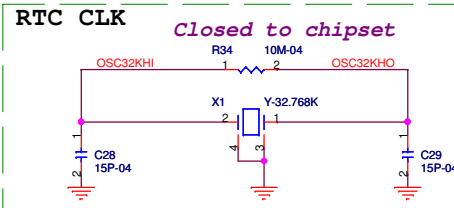
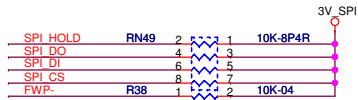
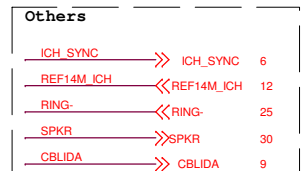
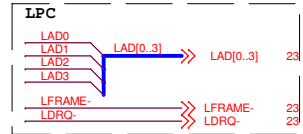
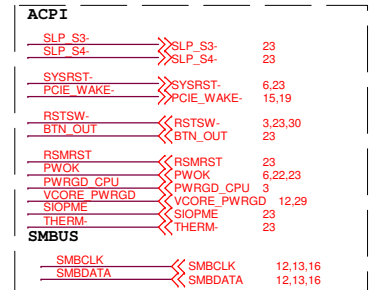
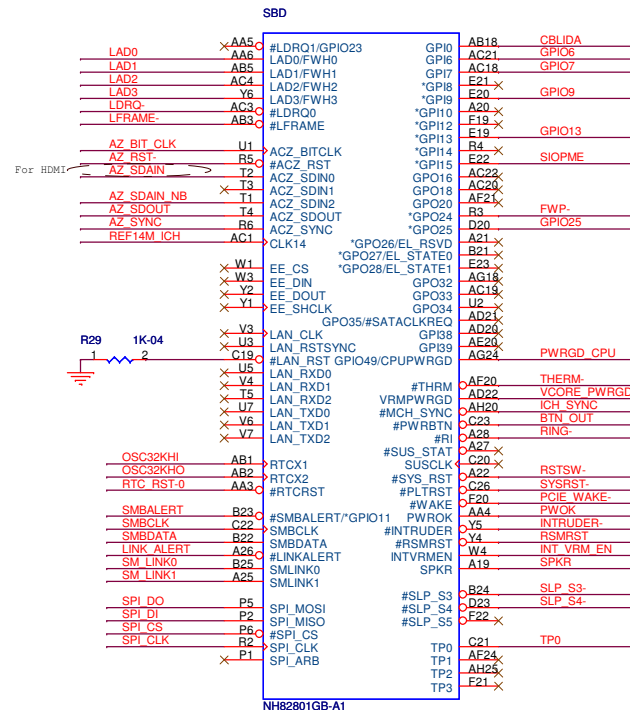
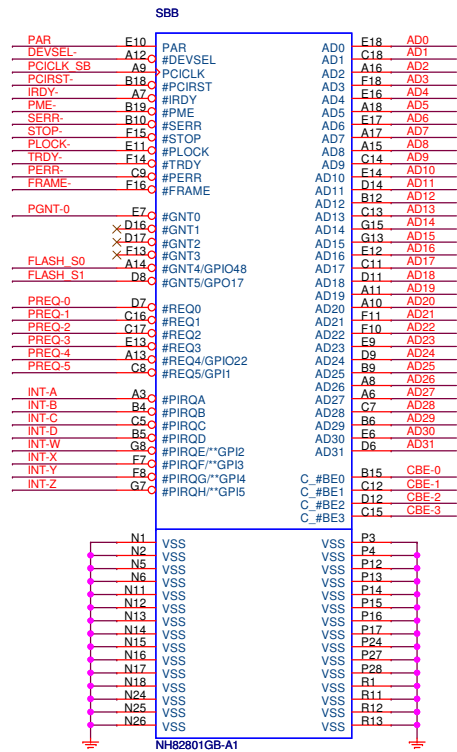
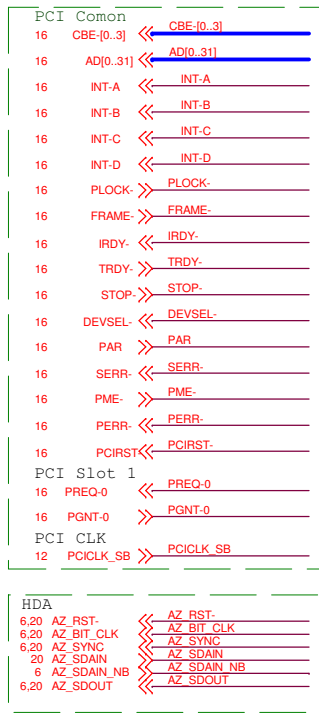
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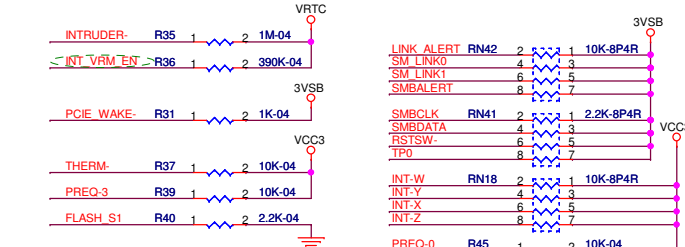








Strap to Enable
Internal SUS VRM



FLASH_S1	FLASH_S0	Flash Cycle
0	1	SPI
1	0	PCI
1	1	LPC

	H	Floating	DESCRIPTION
AZ_SDOUT	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select
AZ_SYNC	PCIE 4x *1	PCIE 1x *4	PCIE 1x/4x Select

Elitegroup Computer Systems

Title

10-ICH7_HDA/SPI/PCI/RTC/MISC

Size Custom

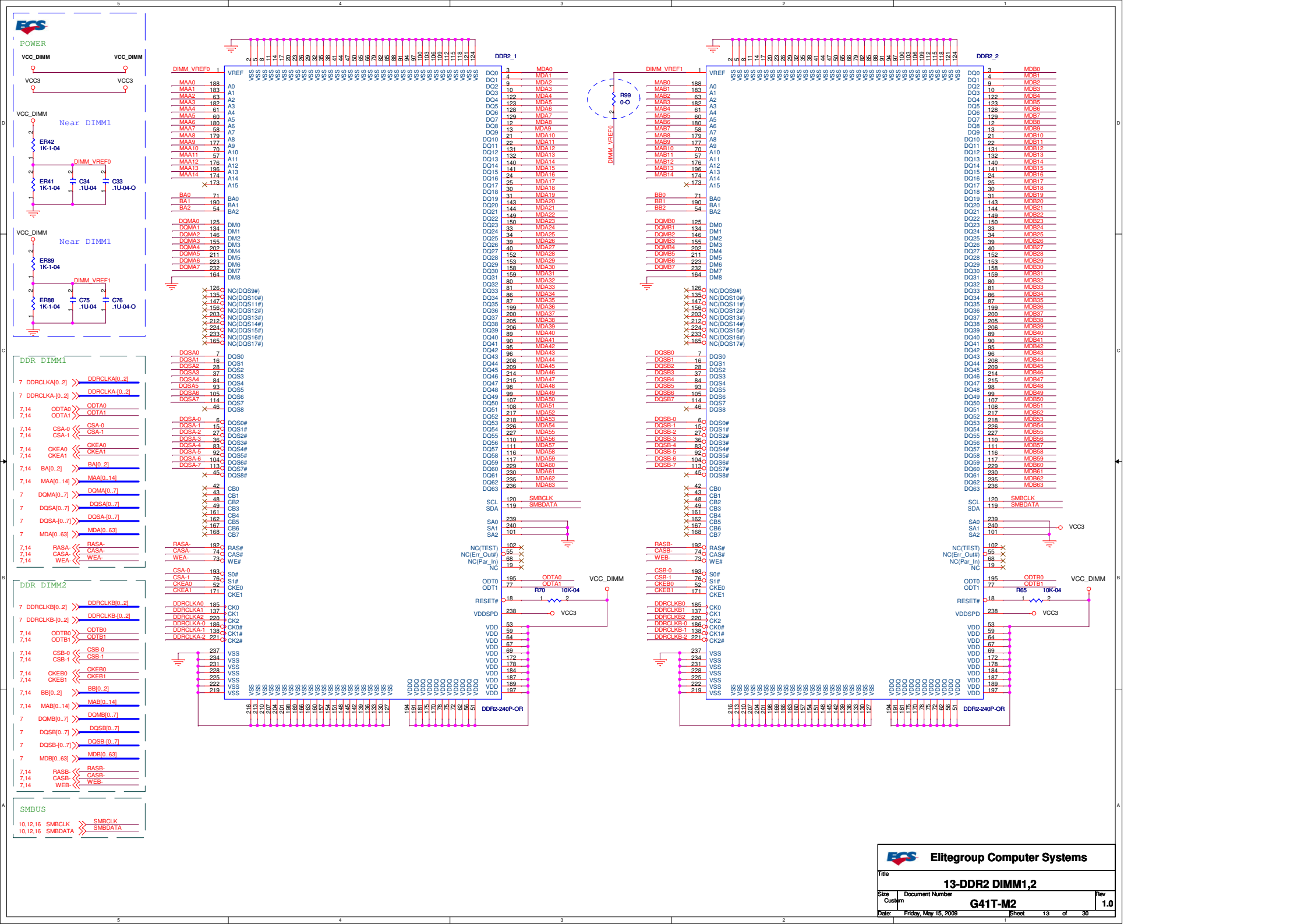
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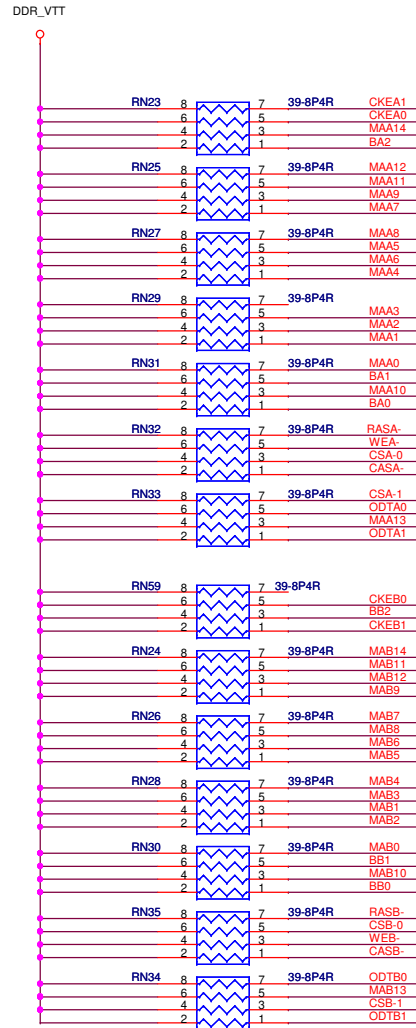
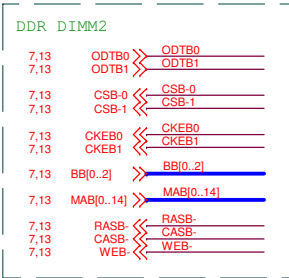
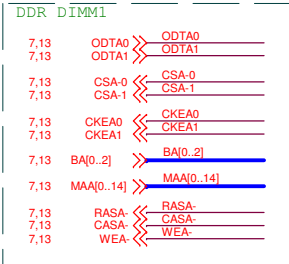
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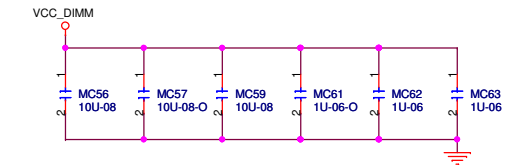
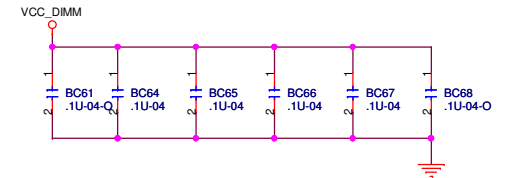
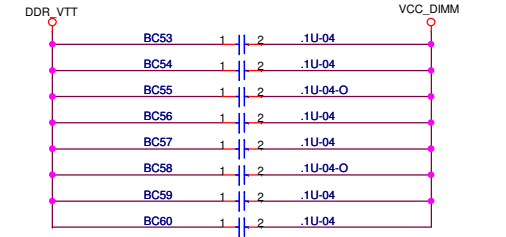
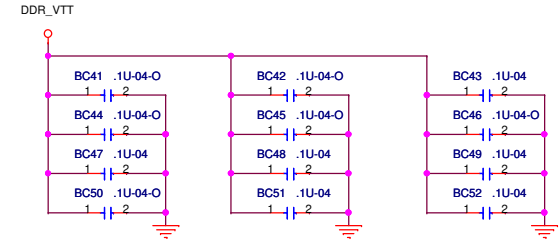
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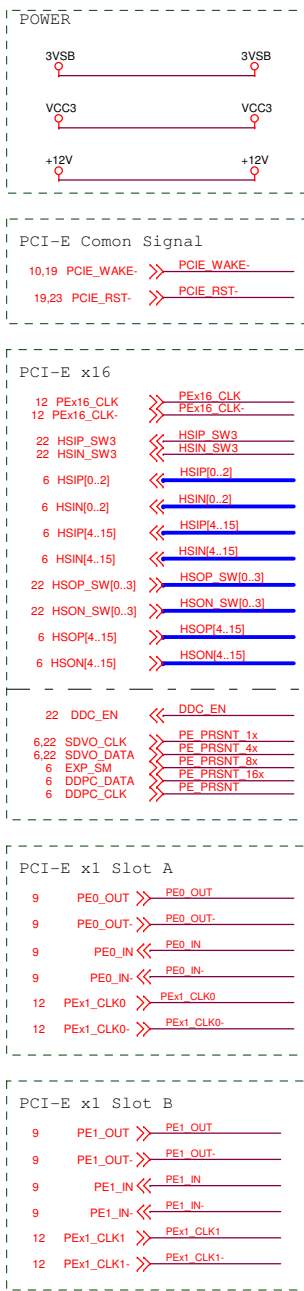
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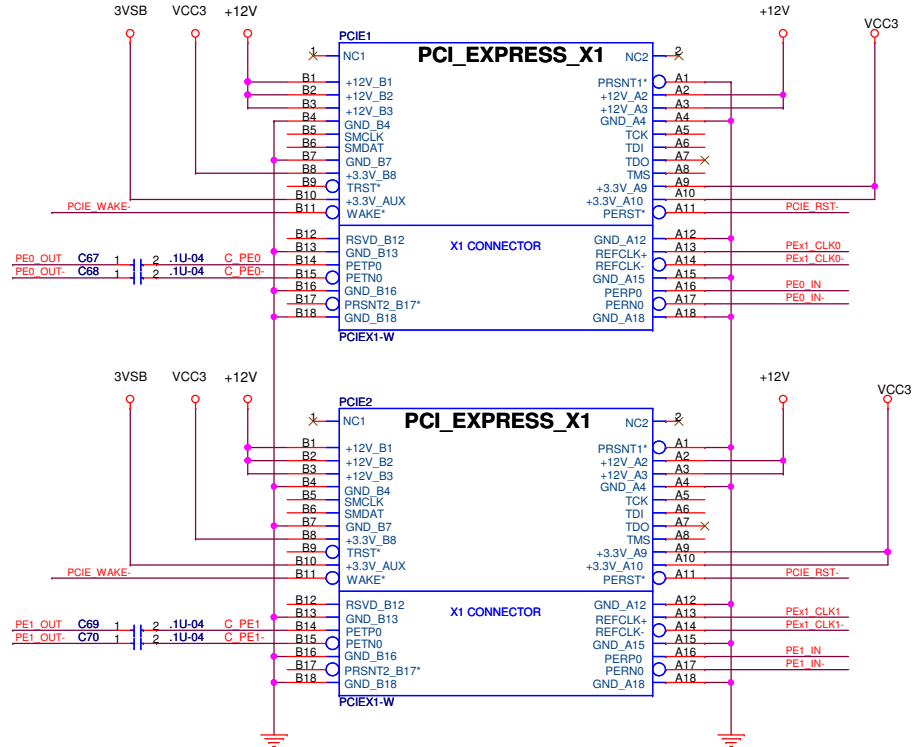
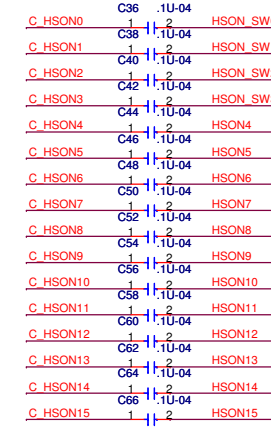
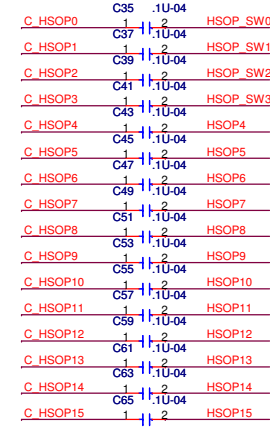
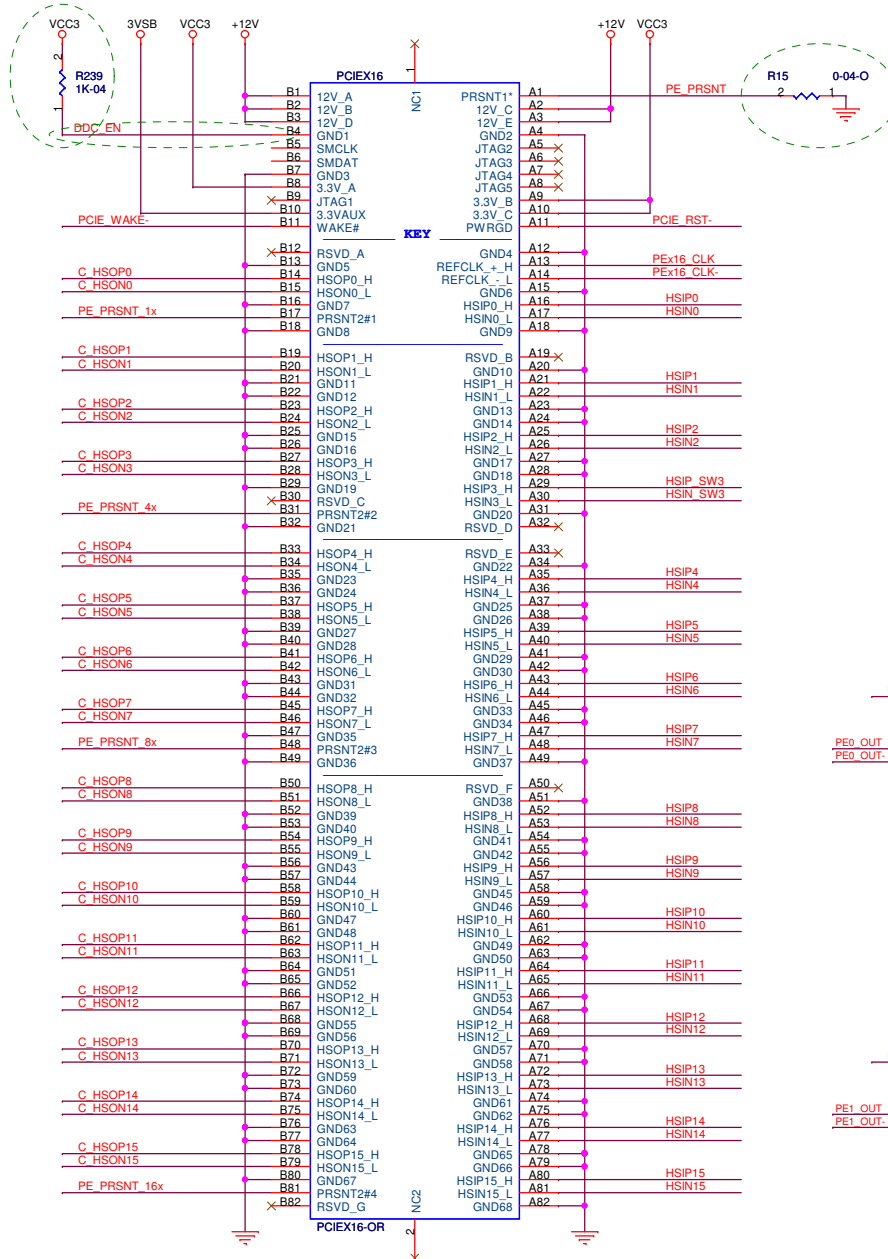
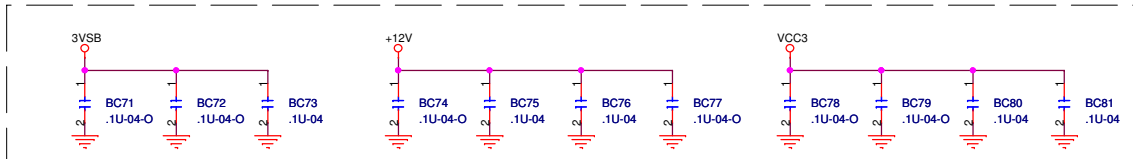


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
Placed within 200mils of VTT Termination R-packs

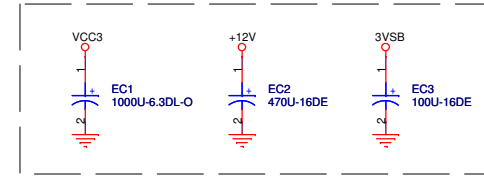




Please place the caps close to PCI-E Slot.



Please place the caps close to PCI-E Slot.



Elitegroup Computer Systems

Title

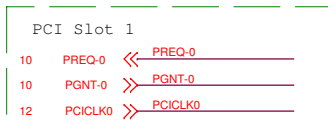
15-PCI-E 16x/1x Slot

Size Document Number

Custom G41T-M2

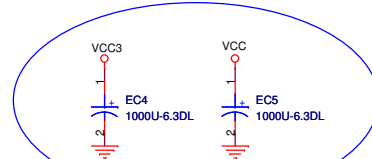
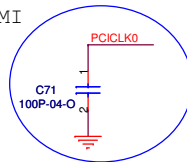
Rev 1.0

Date: Friday, May 15, 2009 Sheet 15 of 30

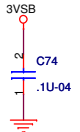
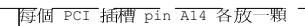
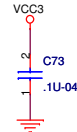
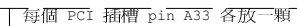
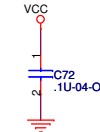
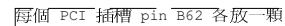
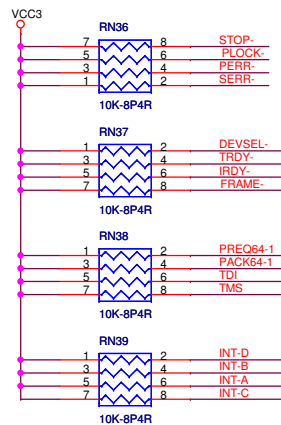


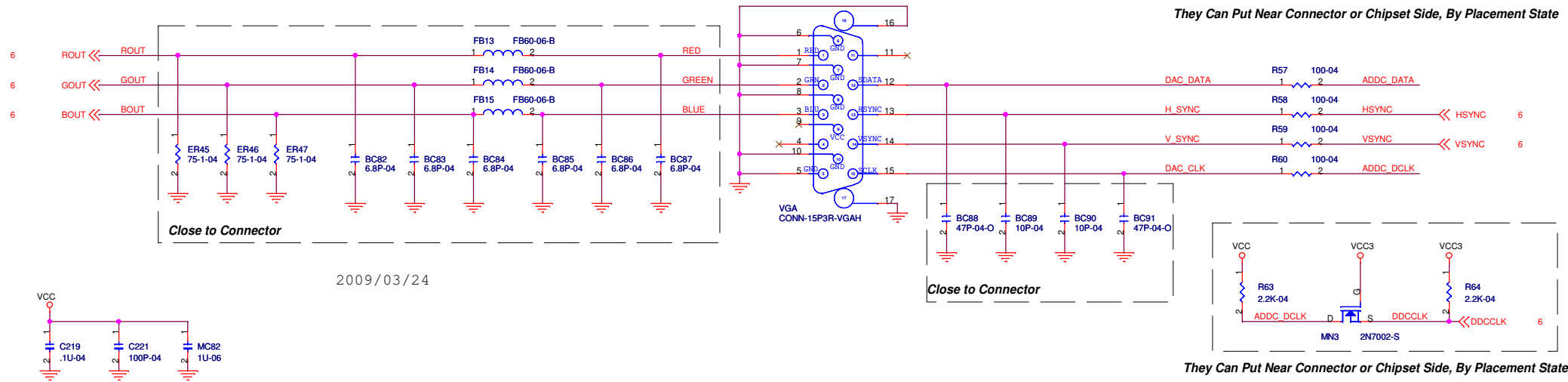
EMI

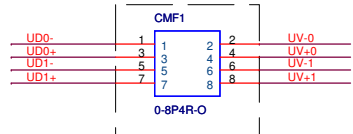
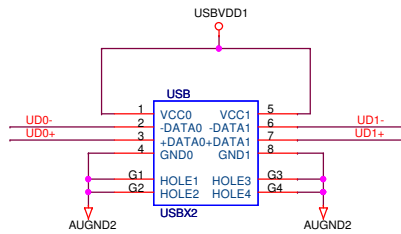
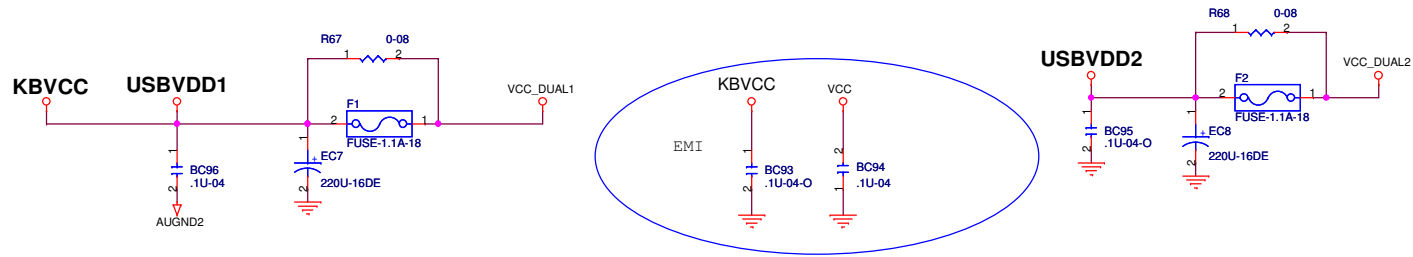
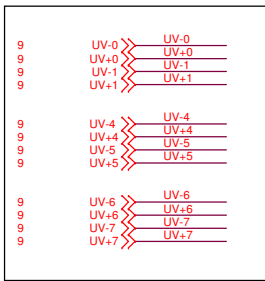
```
IDSEL=AD20
INT [A, B, C, D]
```



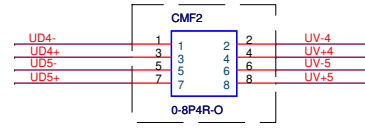
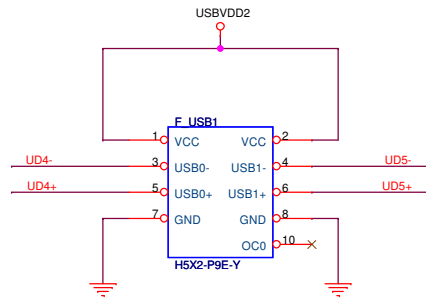
Please place close to PCI1 and PCI2 Slot.



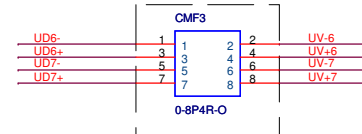
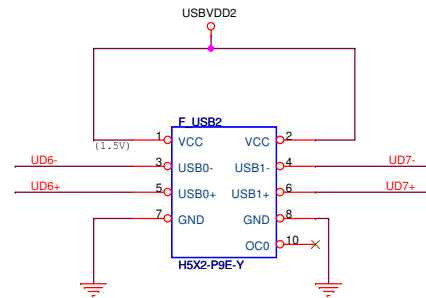




Close to USB connector

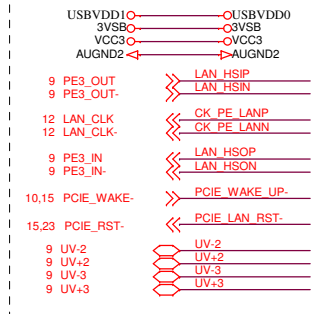


Close to header(F_USB1)



Close to header(F_USB2)

External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.

新手提醒:

- LAN_HSOP/N請接到SB的PCIE RX端
- LAN_HSIP/N請接到SB的PCIE TX端
- LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

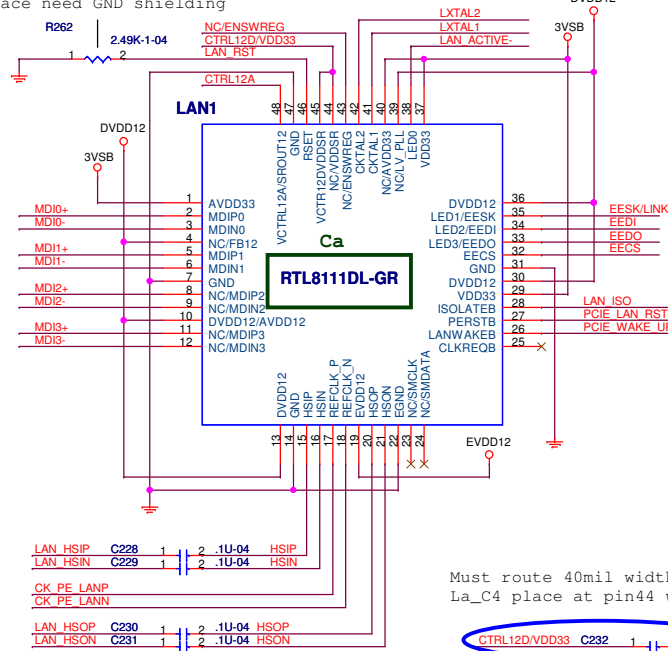
BOM Difference

	RTL8111DL-GR 1000M	RTL8102EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8102EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

Power Difference

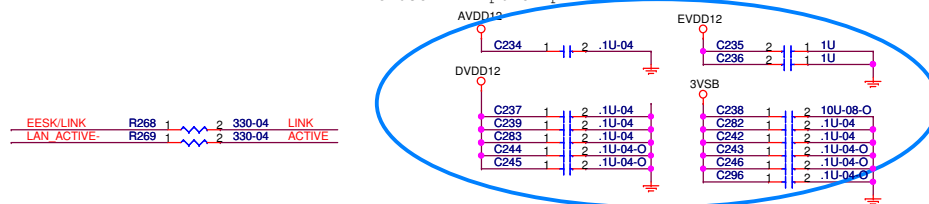
	RTL8111D	RTL8102E
AVDD33	3.3V	3.3V
VDD33	3VSB供應	3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

RSET電阻需close to LAN
Trace need GND shielding

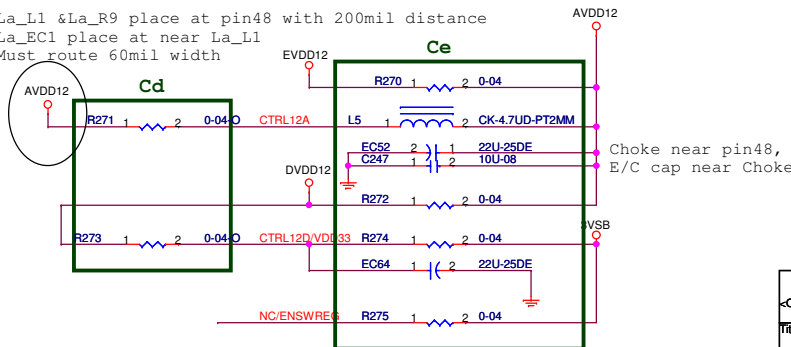
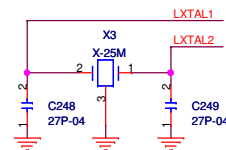


Must route 40mil width
La_C4 place at pin44 with 200mil distance

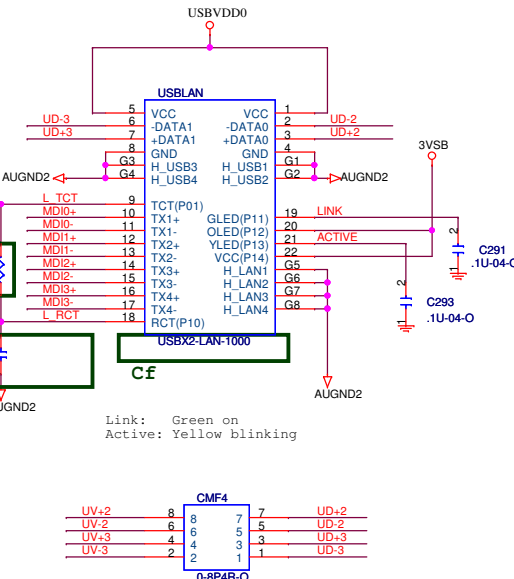
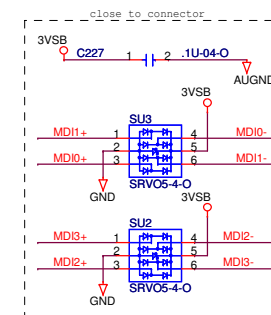
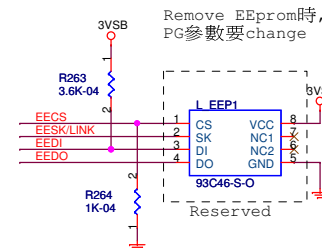
close LAN1 power pin



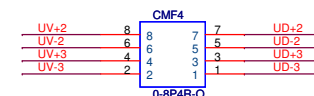
La_L1 & La_R9 place at pin48 with 200mil distance
La_EC1 place at near La_L1
Must route 60mil width



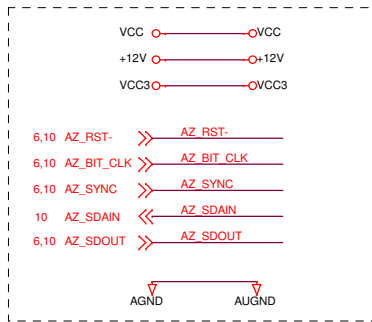
Remove EEprom時,
PG參數要change



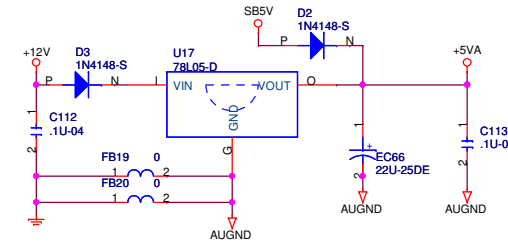
Link: Green on
Active: Yellow blinking



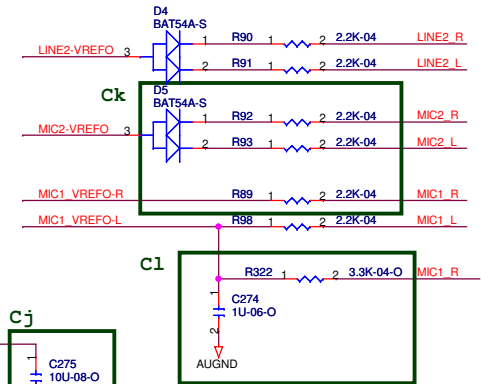
External Connection



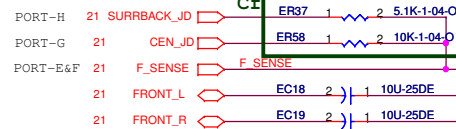
When you found some bug, please inform Ren(ext:665) to update circuit.



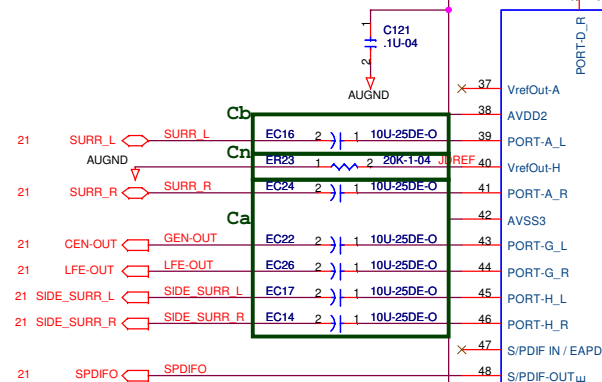
MIC Bias



Resistors Networks



CODEC



ALC662-VC-GR

Place near Chip

Resistors Networks

For ALC662VC

Resistors Networks

For ALC662VC

Resistors Networks

For ALC662VC

Resistors Networks

For ALC662VC

Resistors Networks

For ALC662VC

Resistors Networks

For ALC662VC

Resistors Networks

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Resistors Networks

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Resistors Networks

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Resistors Networks

For ALC662VC

Resistors Networks

For ALC662VC

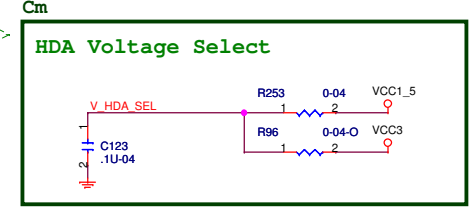
Resistors Networks

For ALC662VC

BOM Difference

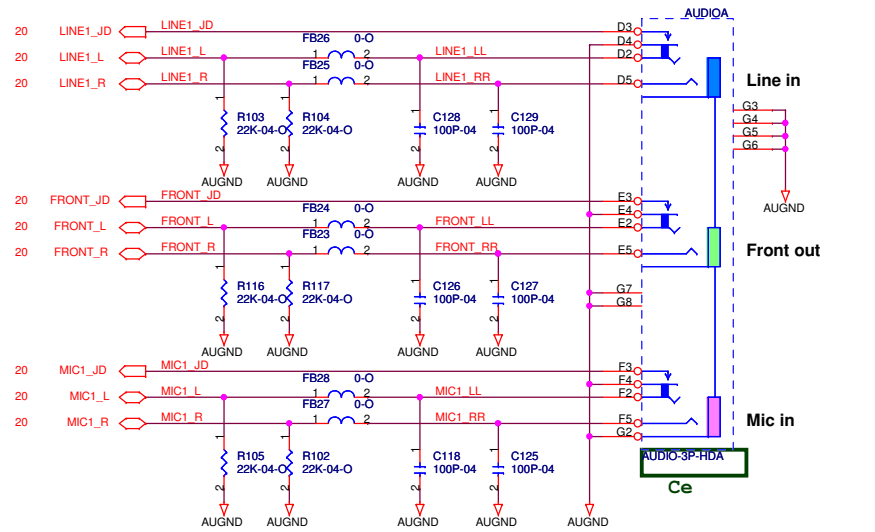
Location	ALC888VC 7.1 Ch	ALC662 5.1 CH	VT1708B 7.1CH	VT1708B 5.1CH
Ca	V	X	V	X
Cb	V	X	V	X
Cc	ALC888-GR C2S	ALC662-VC-GRS	VT1708BS	VT1708BS
Cd	V	X	V	X
Ce	AUDIO-6P	AUDIO-3P-HDA	AUDIO-6P	AUDIO-3P-HDA
Cf	V	X	V	X
Cg	V	X	V	X
Ch	V	X	V	X
Ci	V	V	X	X
Cj	X	X	V	V
Ck	V	V	X	X
Cl	X	X	V	V
Cm	VCC1.5/VCC3	VCC1.5/VCC3	VCC3	VCC3
Cn	20K-1-04	20K-1-04	5.1K-1-04	5.1K-1-04

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

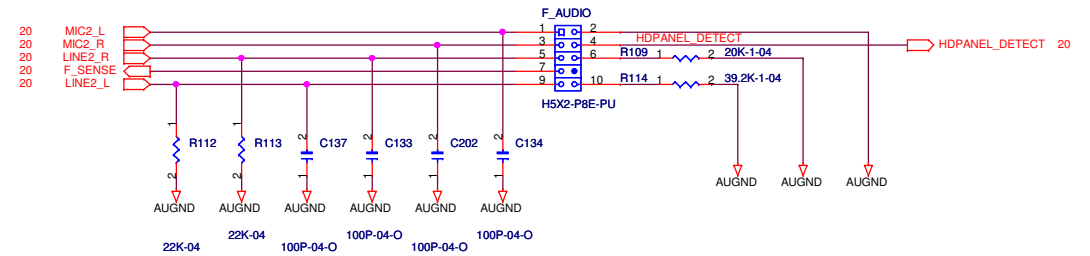


Elitegroup Computer Systems	
Title: 20-Audio Codec (ALC662VC/883/888)	
Size: Custom	Document Number: G41T-M2
Date: Friday, May 15, 2009	Sheet: 20 of 30

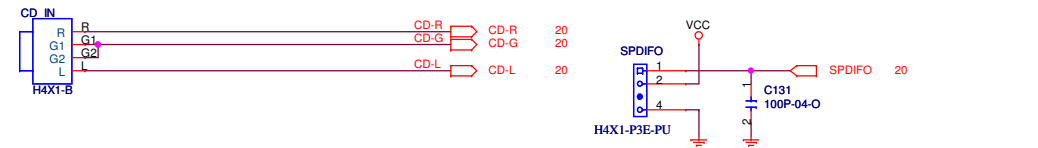
REAR-AUDIO



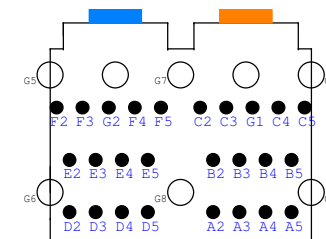
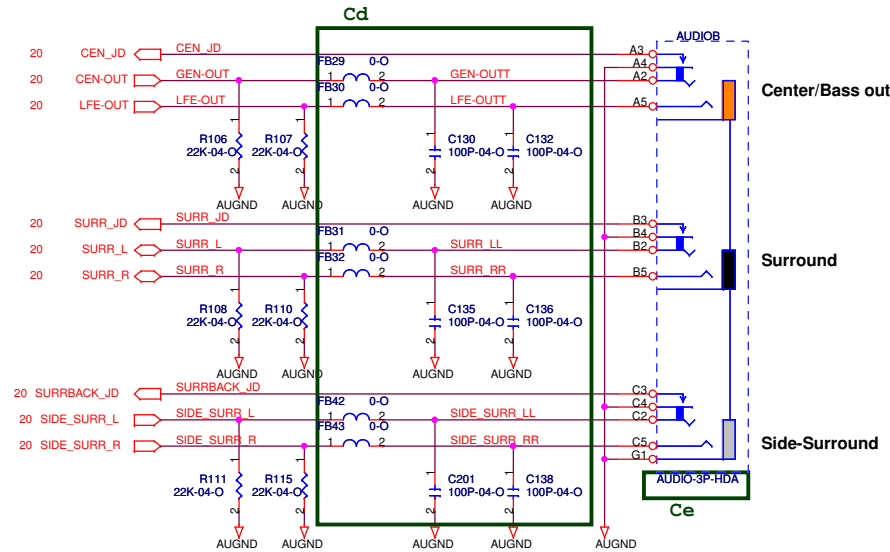
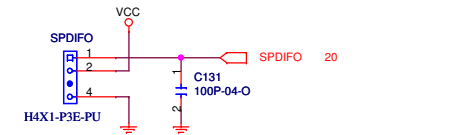
FRONT-AUDIO



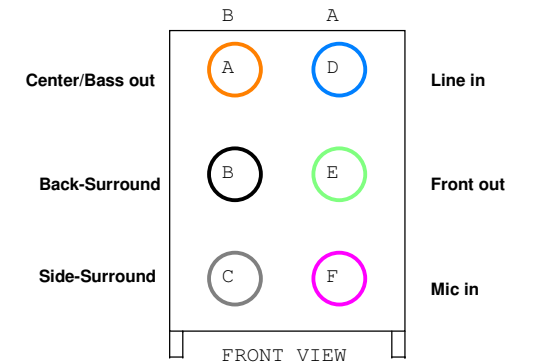
CD_IN



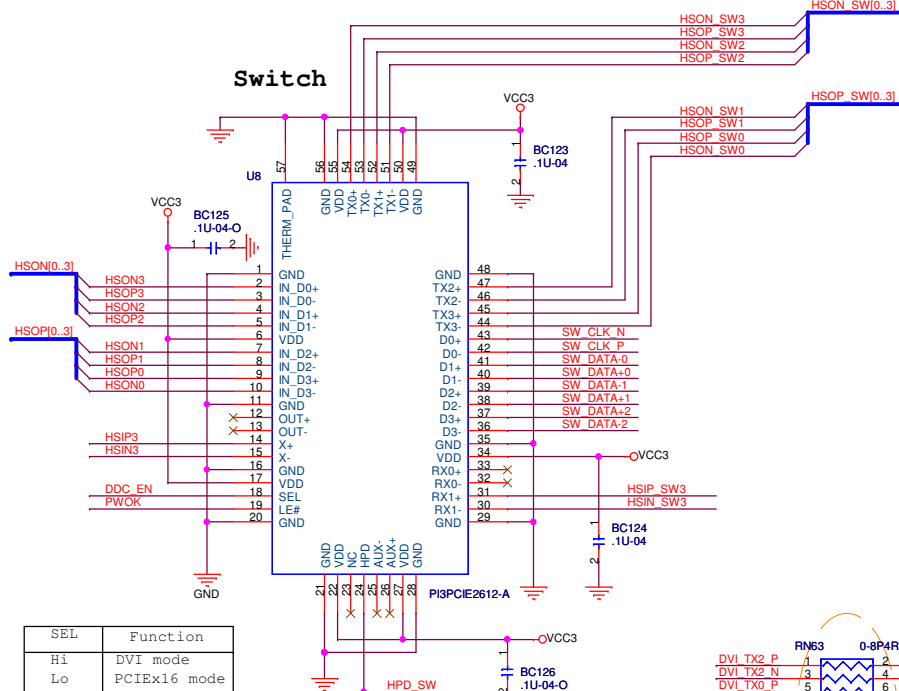
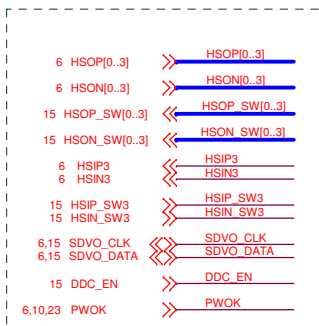
SPDIF-OUT



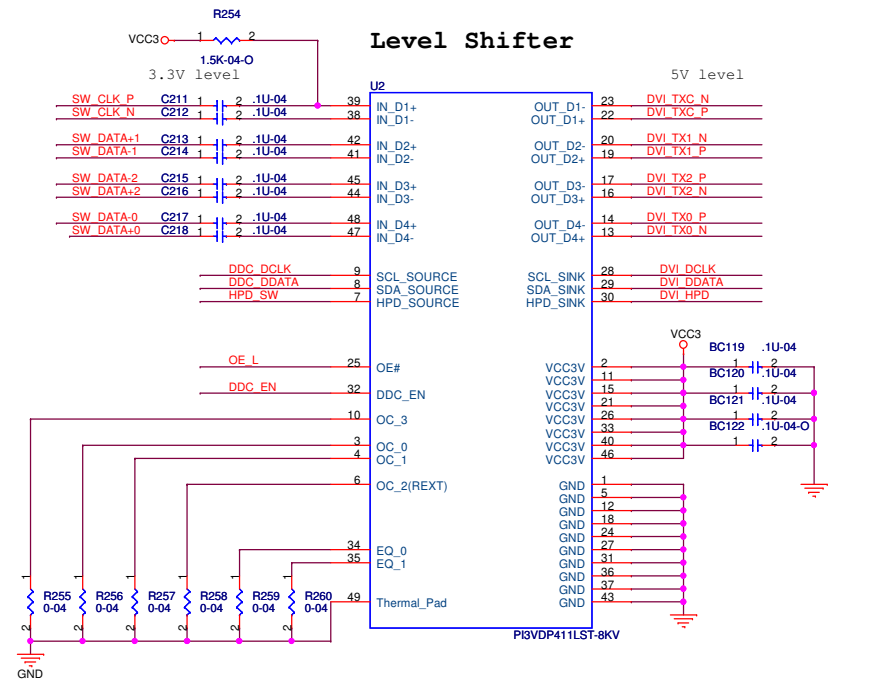
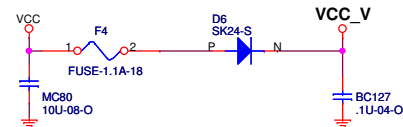
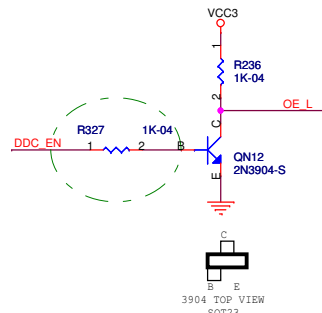
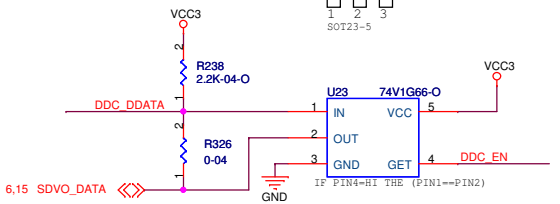
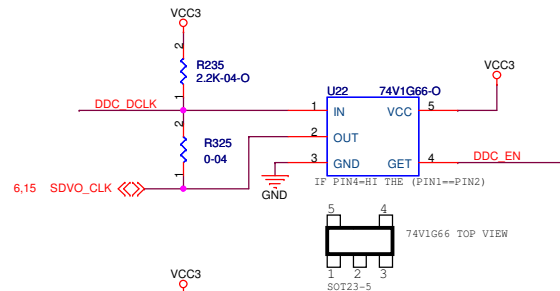
TOP VIEW



FRONT VIEW



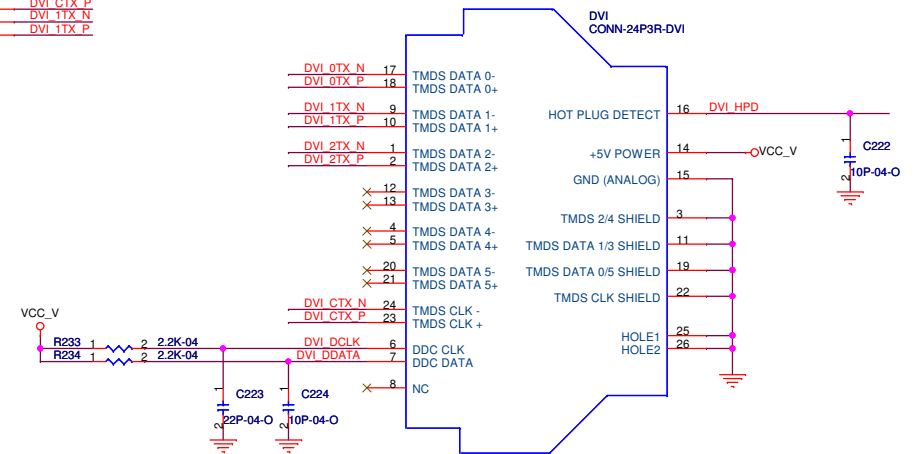
SEL	Function
Hi	DVI mode
Lo	PCIEx16 mode



DDC_EN	Passgate
3.3V	Enable
0	Disable

HD_HPDI	Status
Hi	Plugged
Lo	unplugged

HD_HPDI:Internal 100K pull low

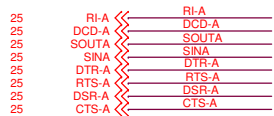


HW Monitor

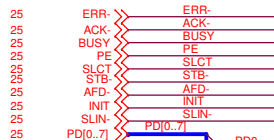


VIN0 for VCORE
VIN1 for V_DIMM
VIN2 for VCC

COM



LPT



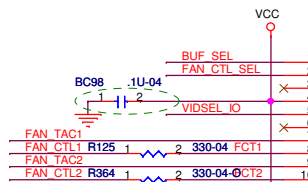
KB/MS



IT8713Power On Strapping Options

JP1	Flashseg1_EN	1	Disabled.
Pin 121		0	Flash I/F Address Segment 1 is enabled
JP2	VIDO_EN	1	Disable VID output pins
Pin 122		0	Enable VID output pins
JP3	CHIP_SEL		Chip selection in Configuration
Pin 124			
JP4	BUF_SEL	1	Output Buffer of PCIRST are open-drain
Pin 1		0	Output Buffer of PCIRST are push-pull
JP5 : JP7	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 00h
Pin 2 & 46		10	The default value of EC Index 15h/16h/17h is 40h
		01	The default value of EC Index 15h/16h/17h is 20h
		00	The default value of EC Index 15h/16h/17h is 7Fh
JP6	VID_SEL	1	Threshold V of VID is 2.0/0.8 V
Pin 5		0	Threshold V of VID is 0.8/0.4 V
JP7	WDT_EN	1	Disable WDT to rest PWROK
Pin 46		0	Enable WDT to rest PWROK

DCD-A
RFA
CTS-A
DTR-A
RTS-A
DSR-A
SOUTA
SINA

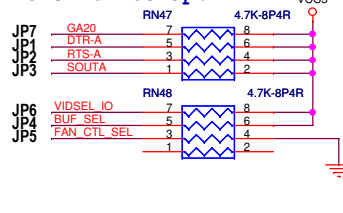


EX_GPIO_2
EX_GPIO_1
EX_GPIO_0
THERM
GTL_SEL2
GTL_SEL1
ACPILED
PWRLED

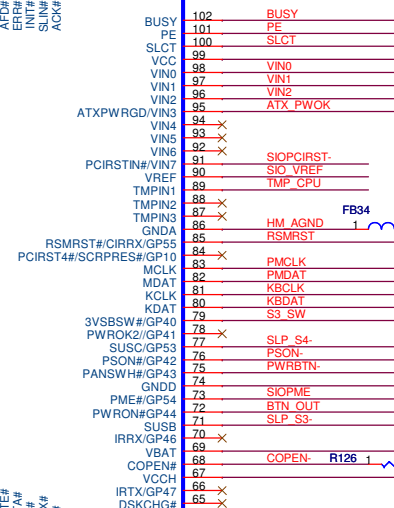
RSTSW-
IDE_RST-
PWOK
PCIE_RST-
SIOPCIRST-
LDRQ-

BC102 1 2 10P-04-O
BC103 1 2 10P-04-O

Power On Strap.



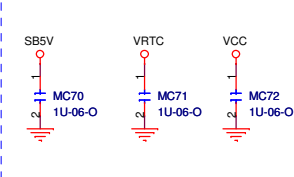
IT8713F-S/JX-L



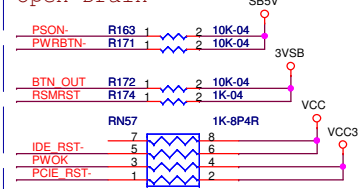
PCIRSTIN#/VIN7
VREF
TMPIN1
TMPIN2
TMPIN3
GND
RSMRST#/CIRRX/JP55
PCIRST4#/SCRPPRES#/GP10
MCLK
MDAT
KCLK
KBDAT
KDAT
3VSBW#/GP40
PWROK2#/GP41
SUSCK/JP53
PSON#/GP42
PANSWH#/GP43
GND
PME#/GP54
PWRON#/GP44
IRRX/JP46
VBAT
COPEN#
VCC
IRTX/JP47
DSKCHG#

PCIE_RST-
SIOPCIRST-
LDRQ-
SIO_CLK
SIO_CLK

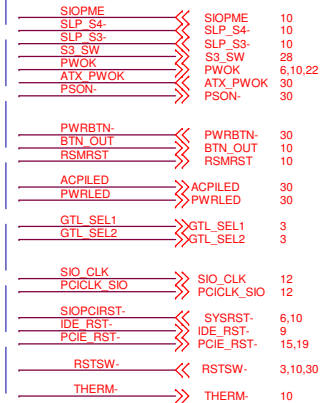
Place Near To SIO Power Pin



Open Drain

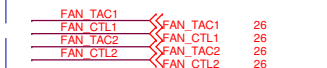


ACPI & Others

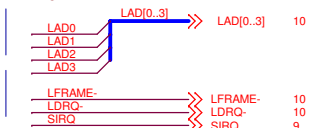


PECI
PECI

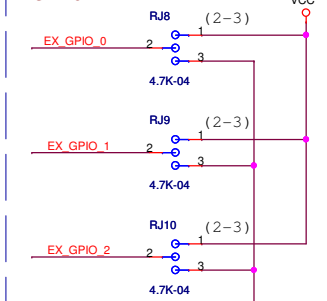
SMART FAN



LPC



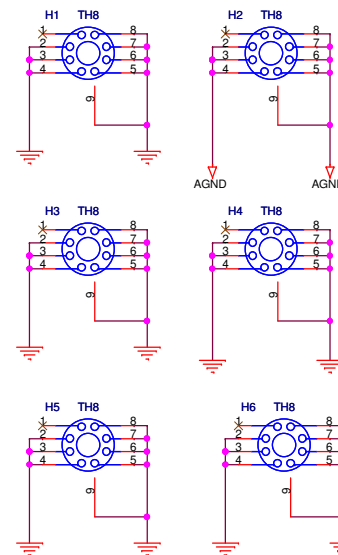
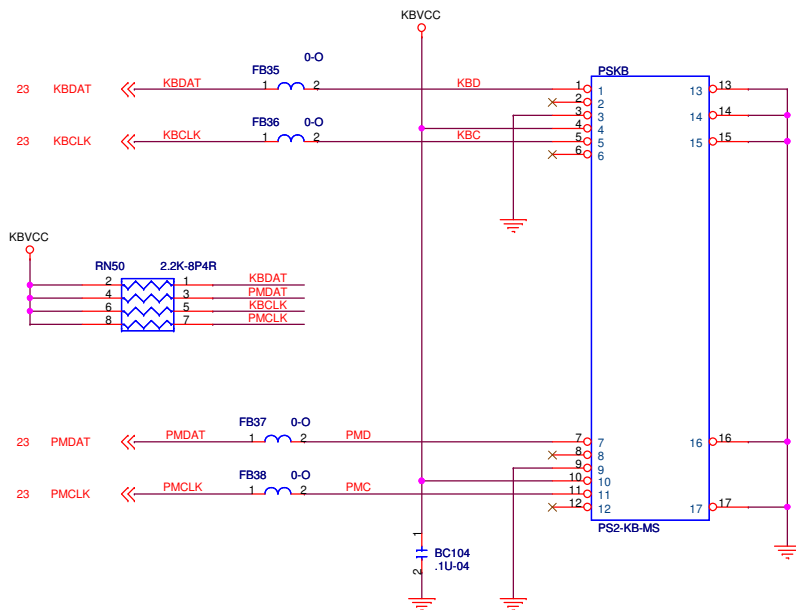
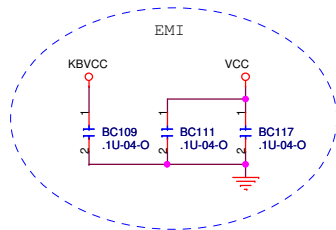
GPIO



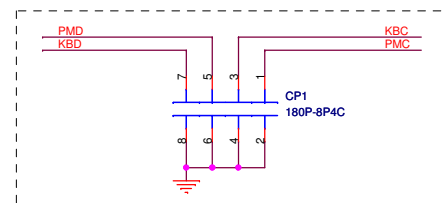
EX_GPIO_0 = 0 -> LPT HW Enable
EX_GPIO_0 = 1 -> LPT HW Disable

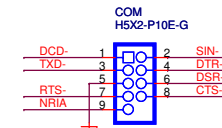
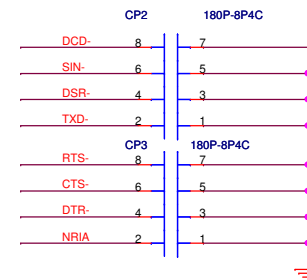
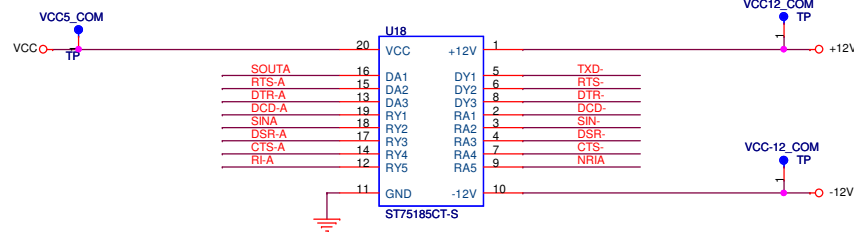
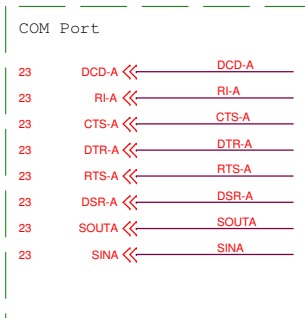
Elitegroup Computer Systems

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PLACE NEAR CONNECTOR

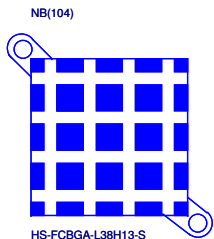




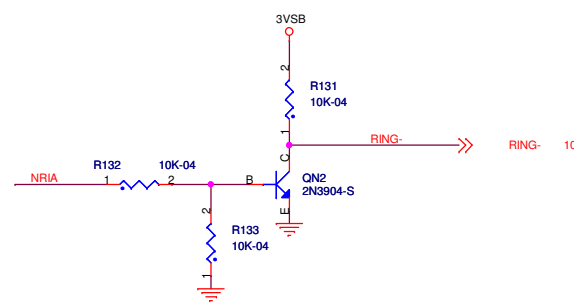
For 104



For 103



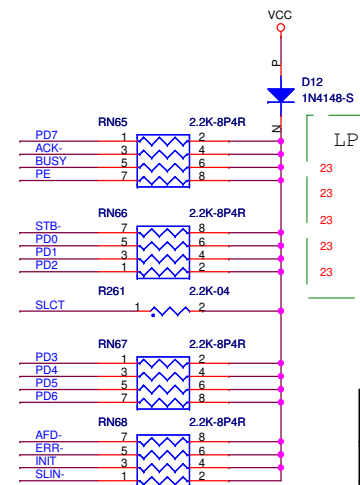
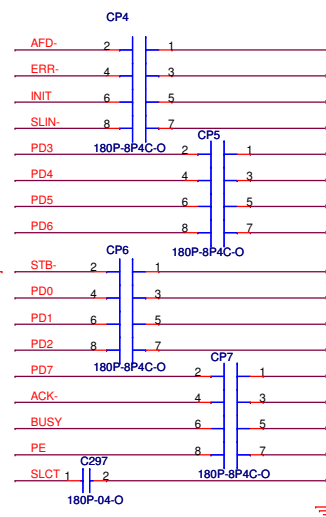
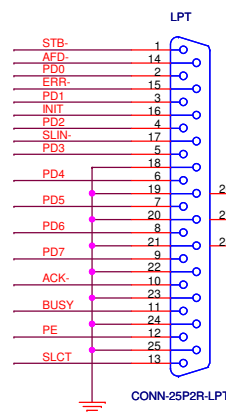
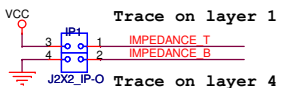
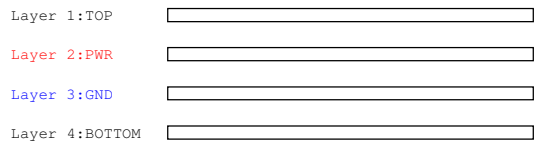
If need 25mm height :
20-120-010937 or 20-120-011420

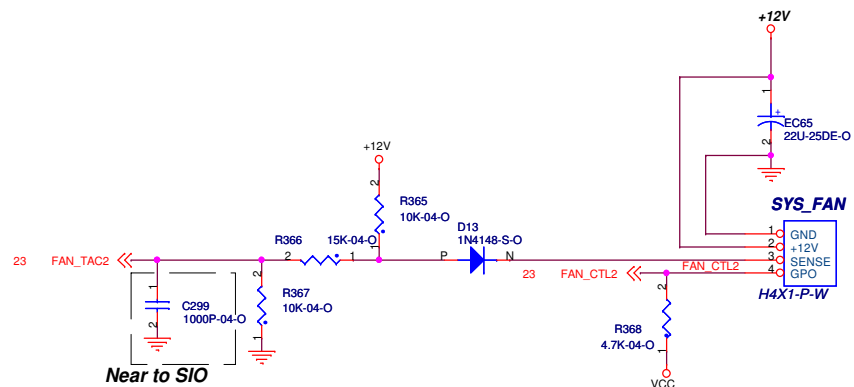
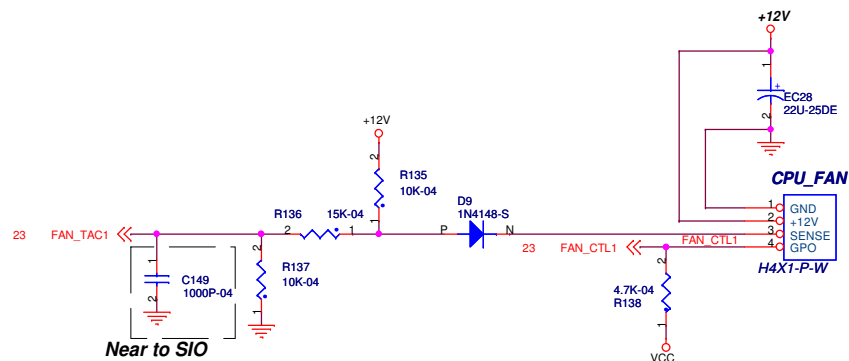


PCB Impedance control

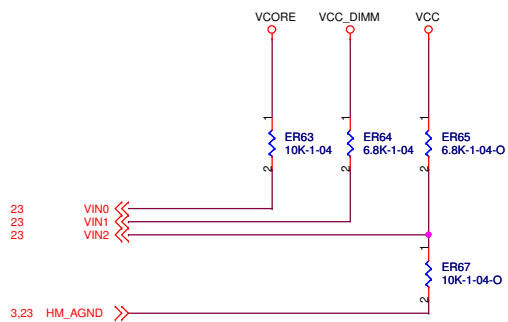
Impedance (ohm)	Trace Width (mil)	Trace Length (S/W/S)	Pre-preg
60	5	(20/5/20)	2116
50	4	(50/4/50)	1080
42	6	(50/6/50)	1080

1)Circuit type 1



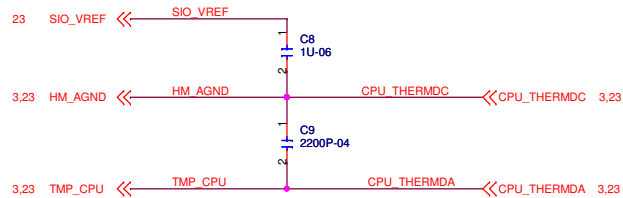


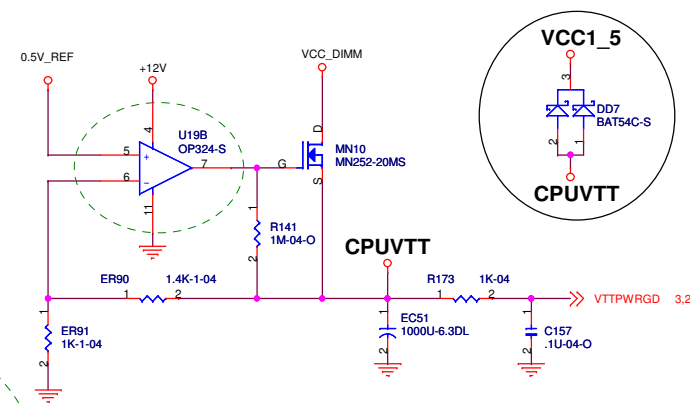
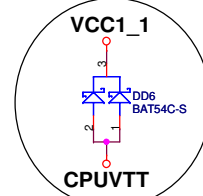
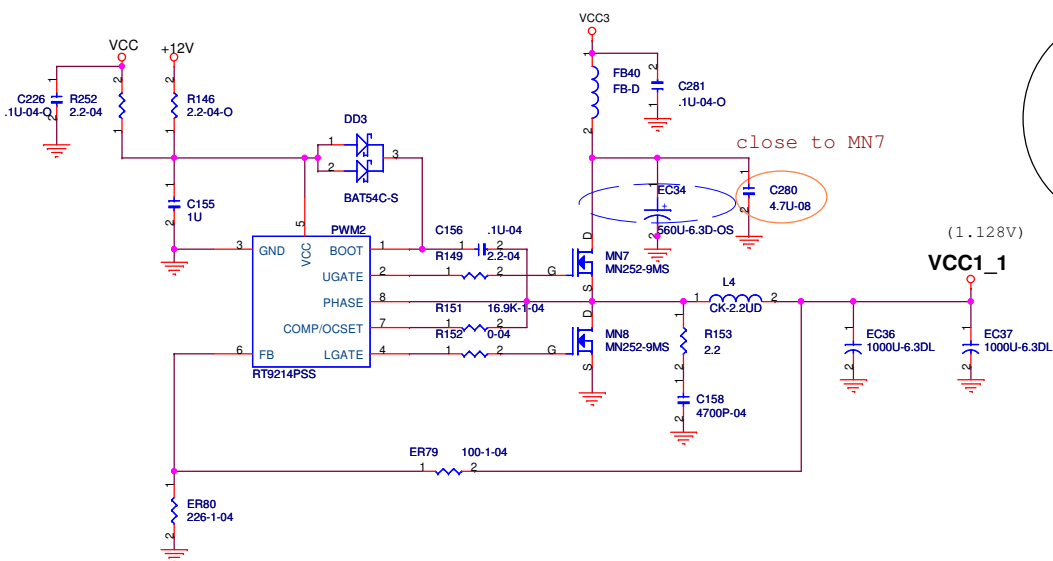
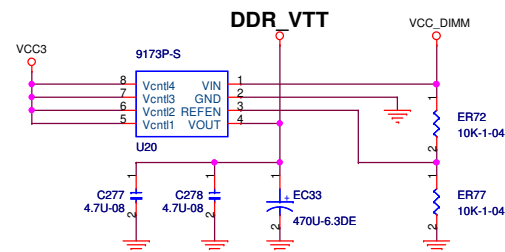
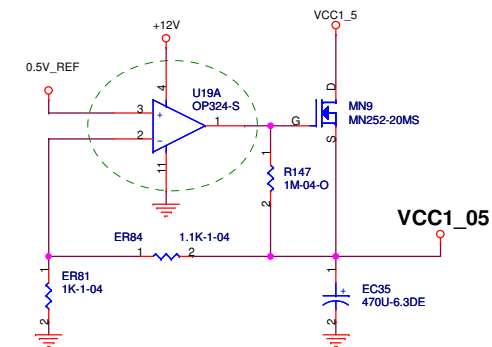
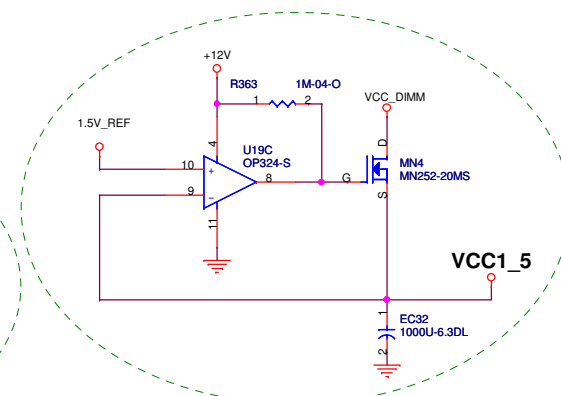
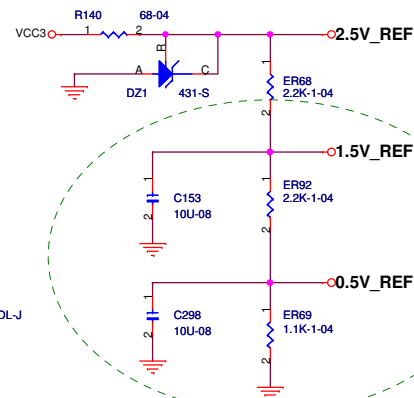
Voltage Monitor

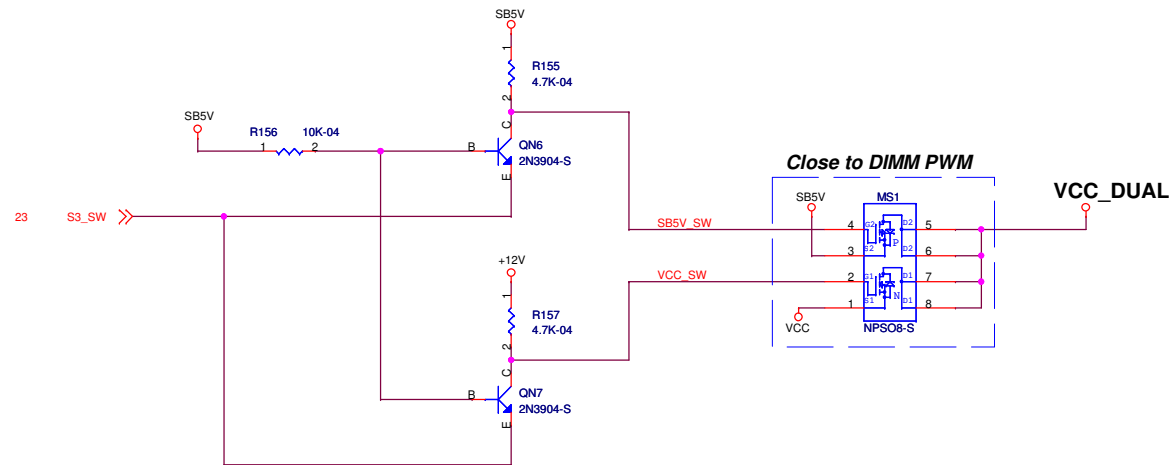
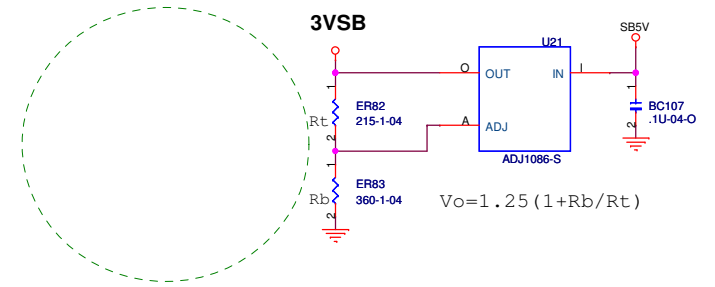
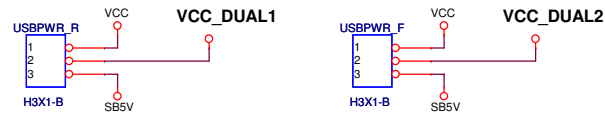


Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode







Memory Power Output Control

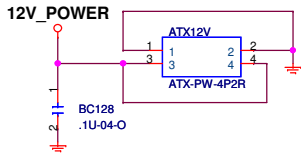
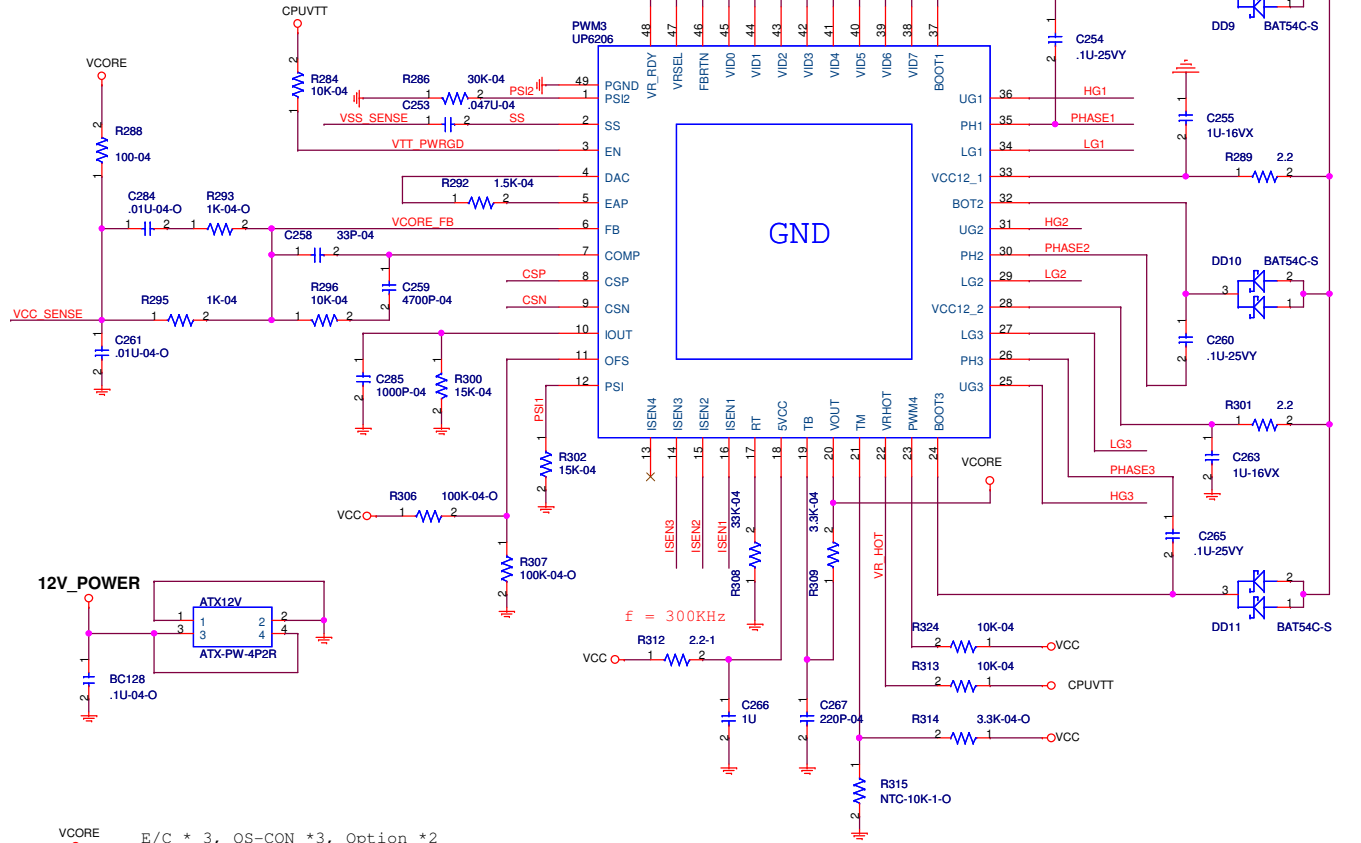
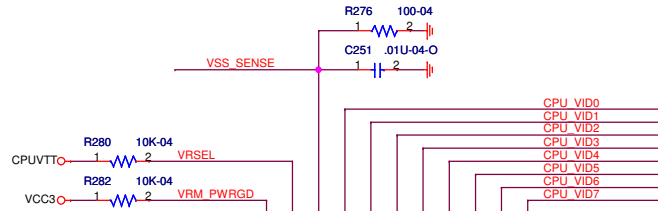
	<i>VCC_DUAL</i>	<i>ATX_PWOK</i>	<i>SLP_S4-</i>	<i>SLP_S3-</i>	<i>S3_SW</i>
<i>S0</i>	<i>VCC</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>
<i>S1</i>	<i>VCC</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>
<i>S3</i>	<i>SB5V</i>	<i>0</i>	<i>1</i>	<i>0</i>	<i>0</i>
<i>S4</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>1</i>
<i>S5</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>1</i>

External Connection

VCC
VCORE
CPUVTT

VCC
VCORE
CPUVTT

3 CPUVID[0..7] >> CPU_VID[0..7]
3 VCC_SENSE >> VCC_SENSE
3 VSS_SENSE >> VSS_SENSE
3,27 VTT_PWRGD >> VTT_PWRGD
10,12 VCORE_PWRGD >> VRM_PWRGD



VCORE E/C * 3, OS-CON *3, Option *2

